A NON-ISOLATED SINGLE PHASE UPS TOPOLOGY WITH 110V/220V INPUT OUTPUT VOLTAGE RATINGS

Carlos G. C. Branco[1], Cícero M. T. Cruz[2], René P. Torrico-Bascopé[2], Fernando L. M. Antunes[2]

[1]Centro Federal de Educação Tecnológica do Piauí
Núcleo de Pesquisas em Engenharia Elétrica
Praça da Liberdade, Nº 1597 – Centro, CEP: 64.000-040,
Teresina-PI-Brasil
E-mail: cgustavo@ieee.org

[2]Universidade Federal do Ceará
Departamento de Engenharia Elétrica
Campus do Pici, Bloco: 705, CEP: 60.455-760, Caixa Postal
6001, Fortaleza-CE-Brasil
E-mails: {cicero, rene, fantunes}@dee.ufc.br

Abstract – **A circuit configuration of a single phase non-isolated on-line uninterruptible power supply (UPS) with 110V/220V input output voltage ratings is proposed, allowing the bypass operation without a transformer even if the input voltage is different of the output voltage. The converter consists of an AC-DC/DC-DC three level boost converter combined with a double half bridge inverter. In this type of configuration size, cost and efficiency are improved due to reduced number of switches and batteries, as well as no low frequency isolation transformer is required to realize bypass operation because of the common neutral connection. Both stages of the proposed circuit operate in high frequency, using a passive non-dissipative snubber circuit in the boost converter and IGBTs switches in the double half bridge inverter, with low conduction losses, low tail current and low switching losses. Principle of operation and experimental results for a 2.6kVA prototype are presented to demonstrate UPS performance.**

Keywords – **Common Neutral Connection, On-Line UPS Systems, Power Factor Correction, Soft Commutation, Transformerless UPS.**

I. INTRODUCTION

Uninterruptible power supplies (UPSs) are being widely used to supply clean and reliable power to critical loads, such as: medical systems, computers, network servers, communication systems and industrial processes. They also protect sensitive loads against power outages under any normal or abnormal utility power conditions. Among different types of UPS systems, the on-line UPS is the superior topology in performance, power conditioning and load protection.

In the conventional on-line UPS configuration, consisting of a boost rectifier/PFC, battery bank, an inverter, and a static switch (bypass). It is normally required an isolating transformer for proper operation of the bypass circuit and also to improve reability of the system during failures or overload. This isolation transformer when operating at the grid frequency has size and cost considerable.

Other topologies proposed to overcome this problem, to place the transformer in a high frequency DC link [1-3]. Although this UPS topology incorporating a high frequency transformer reduces weight of the system, it has increased the number of active switches, compromising the system overall efficiency and reability.

Transformerless UPS incorporating common neutral bus line using half-bridge converter and inverter in both AC/DC and DC/AC conversions, has attracted special interest for applications in computer and telecommunication systems. This type of circuit is highly cost-effective and acceptable due to its total power conversion efficiency improvement and volume and weight reduction [4-6]. However, with conventional boost chopper circuits, higher step-up ratio lowers the boost efficiency. For that reason a new boost chopper circuit configuration, seen in Fig. 1, has been proposed in [7]. Although this topology have offered a way to reduce battery bank size, step-up ratio and capacitors unbalance, it has some disadvantages such as: AC-DC and DC-AC converters switches are exposed to total DC link voltage, larger reactive power flows during rectifier operation and the bidirectional boost-chopper inductor is larger than the one used in normal mode.

The single phase three-level rectifier with a half bridge inverter can be advantageous for many applications [8]. In this converter only half of the DC link voltage is applied across the rectifier switches and the current flows simultaneously through two or three power semiconductors only. Therefore this converter presents less conduction losses, and a common neutral bus line is connected between the middle point of DC capacitors link and load, making it possible to realize the bypass operation without an isolating transformer. This topology has a disadvantage in battery powered mode, because it does not provide a path to charge the two DC link capacitors separately, resulting in DC link capacitors voltage unbalance for some types of load connected to the inverter.
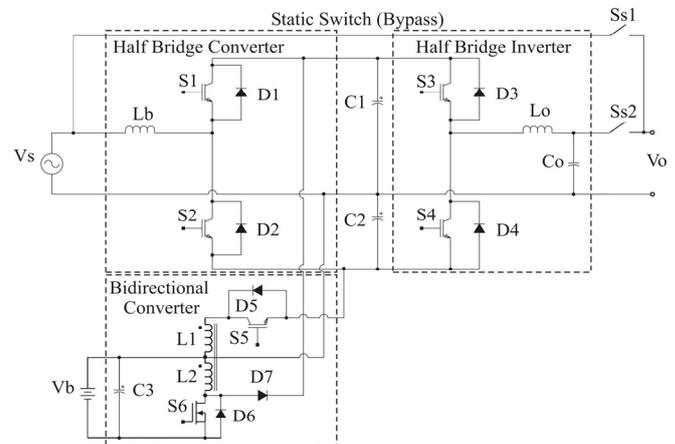
Fig. 1. Single phase UPS based on half bridge converter-inverter and a buck-boost chopper circuit.
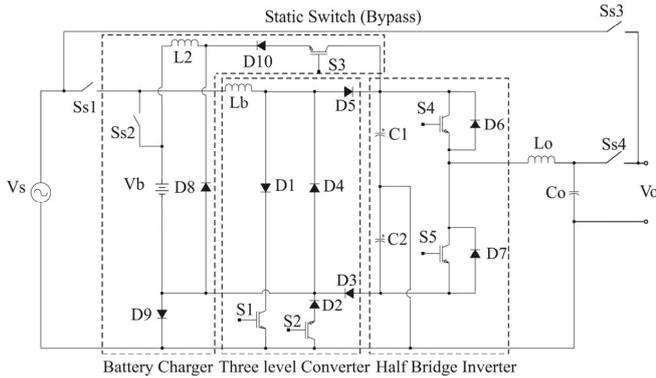
Fig. 2. Modified three level rectifier with half bridge inverter scheme.

Fig. 2 shows a modified single phase three level rectifier and a half bridge inverter scheme reported in [9-10], with a battery set and static switches arrangement that overcome the drawbacks related above.

The main advantages of this configuration are the possibility to correct the DC link capacitors voltage unbalance, reduce both step-up ratio of the boost converter and the number of battery units necessary for the battery powered operation mode and the use of fewer active switches compared to topologies presented in [4-7].

Topologies with a common neutral PWM boost rectifier in the front end of the UPS system are characterized as voltage doublers [11] requiring a minimum DC link voltage of 622V for operation of the boost rectifier when the utility voltage is 220Vac. This operating voltage requires higher cost semiconductors and passive components. Moreover, it requires a very high voltage battery bank, which leads to increase storage battery cost and lower reability.

In this paper it is proposed a circuit configuration that combines the advantages of the presented topologies with common neutral connection, three level rectifier and half bridge inverter, and, at the same time it can operate for any input/output voltage (110V/220V) requirements. This configuration can also be extended for the conventional half bridge AC-DC converter and other voltage doublers converters with middle point capacitors.

II. PROPOSED UPS CIRCUIT

A. Topology Description

The schematic of the single phase on-line UPS with universal input output voltage is shown in Fig. 3[12]. Due to the high voltage of the DC link required by the 220Vac utility supply, an autotransformer with three taps provides the operation of the UPS with 110Vac. Using this configuration, it is possible to use the topologies proposed with common neutral connection without increasing to much the system overall cost. The autotransformer is, at least, 50% cheaper and half the weight of the isolating transformer, which is normally bulky and heavy while operating in commercial AC line frequency. That solution makes this UPS topology possible to work in any conventional utility AC voltage (110V/220V).

This scheme also has the capability of supplying two different levels of load voltage. In this system, the two specifications of input voltages fix the two outputs voltages, so that the ratings of output voltages are 110Vac and 220Vac. To achieve this, a double half bridge circuit [13] provides two outputs of 110Vac, each one with half of the total output power of the boost converter.

It is possible to generate a sinusoidal voltage of 110Vac rms at each half bridge inverter leg. By synchronizing the operation of both half bridge inverter legs, it is possible to obtain 220Vac at the output of the UPS as shown in Fig. 3. This is obtained by the sum of the two individual outputs voltages. When using only this tap as load, it could deliver total output power of two half bridge legs.

If there are loads connected to both 110Vac and 220Vac outputs, the system also has the same performance, providing a high quality sinusoidal voltage for each output, sharing output power observing the limit of the power capacity of each 110Vac and 220Vac output. Two separated control schemes, one for each half bridge leg, have been used and will be further explained.

To perform bypass operation, four static switches have been used for connecting AC line directly to the load during system overload or problems with the converters operation. Two additional static switches or electromagnetic contactors
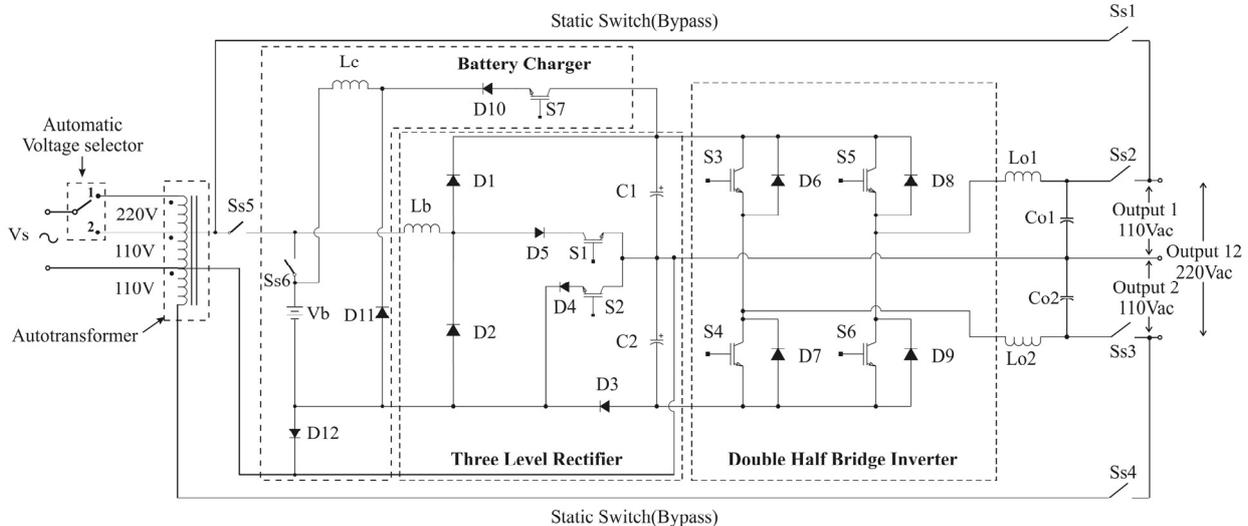
Fig. 3. Proposed non-isolated single phase on-line UPS topology with 110V/220V input output voltage.

are used to commutate between AC line mode and battery mode. A simple buck converter, showed also in Fig. 3, is used to perform battery charging regulation.

B. Principle of Operation

The operation of the proposed UPS can be divided in three modes: the on-line mode, the battery powered mode and the bypass mode.

1) On-Line mode: In accordance with the utility voltage level, an automatic detector sets the UPS for the proper input voltage. For utility voltage of 220Vac, the voltage selector should be put to position 1, allowing the 220V utility voltage across the autotransformer 220V winding, and a tap divides input voltage, providing the boost rectifier with 110Vac. On the other hand, if the utility voltage is 110Vac, the voltage selector should be switched to position 2, whose winding is always supplying the converter with the same input voltage value.

During the on-line operation mode S_{s5}, S_{s2} and S_{s3} are kept on and S_{s1}, S_{s4} and S_{s6} kept off. The control of the three level rectifier operating in the boost mode is realized in such a way to provide an AC line current with low THD and high power factor, while maintaining a constant and balanced DC voltage across the DC link capacitors. The generated current paths and switches states in accordance with Vs of the boost mode operation are shown in Table I.

The double half bridge inverter operates as two synchronized independent half bridges, as well-known in the literature, to produce 220Vac output by the sum of two 110Vac outputs in phase.

2) Battery powered mode: When the supervisory circuit detects AC line failure, switch S_{s5} is turned off and S_{s6} turns on, transferring the input of the boost converter from the AC utility to the battery bank for boost DC/DC operation, which now function as described in Table I.

Accordingly to the control strategy adopted to battery powered mode, the battery bank transfers energy alternatively to each capacitor of the dc link for half period of the utility voltage. V_{bat} represents which capacitor will receive energy during battery powered operation with its respective current path.

TABLE I
Boost Operation Switching States

On-Line operation current path		
Vs cycle	Energy storage in inductor Lb	Energy transfer to DC link
Positive (⌐)	Vs ⇒ Lb ⇒ D5 ⇒ S1 ⇒ Vs	Vs ⇒ Lb ⇒ D1 ⇒ C1 ⇒ Vs
Negative (⌐)	Vs ⇒ S2 ⇒ D4 ⇒ D2 ⇒ Lb ⇒ Vs	Vs ⇒ C2 ⇒ D3 ⇒ D2 ⇒ Lb ⇒ Vs
Battery powered operation current path		
V_{bat}	Energy storage in inductor Lb	Energy transfer to DC link
(C1 Transfer)	Vb ⇒ Lb ⇒ D5 ⇒ S1 ⇒ S2 ⇒ D4 ⇒ Vb	Vb ⇒ Lb ⇒ D1 ⇒ C1 ⇒ S2 ⇒ D4 ⇒ Vb
(C2 Transfer)	Vb ⇒ Lb ⇒ D5 ⇒ S1 ⇒ S2 ⇒ D4 ⇒Vb	Vb ⇒ Lb ⇒ D5 ⇒ S1 ⇒ C2 ⇒ D3 ⇒ Vb

3) Bypass mode: During overload or any problem in the UPS converters, a supervisory circuit detects the fault and sets static switches S_{s1} and S_{s4} to on while S_{s2} and S_{s3} are set to off in order to isolate the failure. This provides zero time transfer ratio. The autotransformer has three taps, two of them to supply the UPS input in 110Vac as mentioned above and the third one is used in the bypass mode, supplying the second half bridge leg output with 110Vac.

C. Control Strategy

The proposed UPS control strategy is achieved with an analog scheme using well-know dedicated integrated circuits and a supervisory circuit based on a 8-bit high performance RISC microcontroller PIC16F870.

1) Three level boost converter control: The three level boost converter operating control scheme for both on-line mode and battery powered mode is shown in Fig. 4. A simple control strategy using UC3854B controller from Texas Instruments is adopted as main controller, to accomplish a low distortion sinusoidal ac line current, using instantaneous average current mode control [14]. An external regulator is used to obtain voltage balance compensation signal to be added to the input current reference. During on-line mode of operation, the current reference signal is obtained from AC line when controller switch mode relay is in position 1.Then in battery operation mode; it is switched to position 2 to provide a symmetric DC reference. To accomplish capacitors voltage balance in battery powered mode, this current waveform reference is necessary. A logic circuit after PWM signal modulator is synchronized by microcontroller and used to provide gating signals for S_1 and S_2 switches in both operations modes.

2) Double half-bridge control: Due to the fact that each half bridge inverter has a separated output, two similar PID controllers were used to provide output voltage regulation. Fig. 5 shows a complete scheme of the inverter's control block. Sinusoidal pulse width modulation technique for the closed loop regulation with a LC filter at the output provides a high quality sinusoidal voltage to any type of load. Bipolar modulation strategy is adopted, applying a two level voltage waveform to the input of LC filter. In the circuit shown in Fig. 5, the reference sine wave generated by the microcontroller is synchronized with the utility and
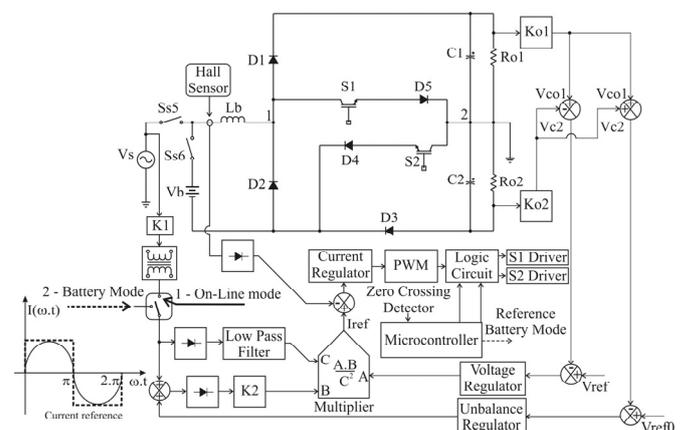
Fig. 4. Three level boost converter control block.
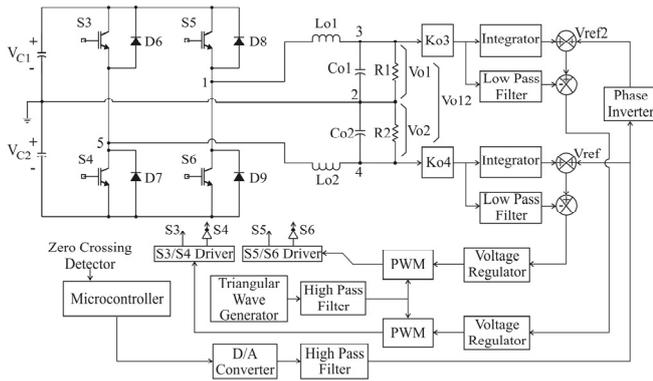
Fig. 5. Double half bridge control block.

compared with the sampled output voltage, so the output voltage is always equal to the reference sine wave of each inverter. The integrator block is responsible for the DC component compensation of the output voltage. The microcontroller with an external D/A converter composed by a R2-R network, generates a sine wave reference synchronized with the utility voltage. The main feature of this control strategy is that the sinusoidal reference voltage for each half bridge controller is delayed 180º from each other in order to provide a sum of the two outputs voltages when supplying the load in 220Vac. If the reference signals are delayed with other angle, the second voltage value resulted by the sum of the two outputs values could be adjusted.

III. PASSIVE NON-DISSIPATIVE SNUBBER CIRCUIT APPLIED IN THE FRONT END CONVERTER

A passive non-dissipative snubber circuit presented in [15] was employed to achieve soft commutation, during turn-on and turn-off in both active switches in three level converter, increasing system overall efficiency in any operation mode and allowing the increase of switching frequency operation of the three level converter.

Fig. 6 shows the turn-on turn-off snubber circuit topology applied to the three level boost converter. The passive components used in each boost diode (D_1 and D_3) are shown within the dashed line. Recovery mechanism in diode D_2 does not need to be minimized because during the negative
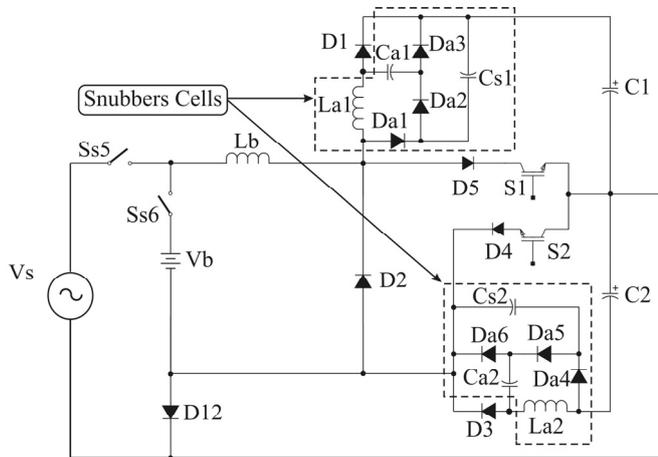
Fig. 6. Passive non-dissipative snubber circuit scheme applied in the three level boost converter.

cycle of the utility, it is conducting (On-line Mode) and during the battery powered mode it is always blocked. A detailed description, operation and design procedure are also presented in [15].

Compared with the utilization of SiC devices in order to minimize boost switches commutation problems, this snubber circuit is very reliable and provides a considerable cost reduction, because it's composed mainly by passive components.

IV. EXPERIMENTAL RESULTS

The proposed non-isolated single phase on-line UPS with 110V/220V input/output voltage design specifications are shown in Tables II, III, IV and V. The switching frequency of both converters was assumed f_s=50kHz.

TABLE II
Developed UPS Specifications

Input voltage	1Ø 110V / 220V ±15%
Output voltage	110V(Vo1, Vo2) / 220V(Vo12)
Commercial Frequency	50 / 60Hz
Output Power Capacity	1.3kVA per Half Bridge Inverter
Input Power Factor	0.99
Output Power Factor	0.7 – 1.0
DC Link Voltage	440V
Number of Batteries (In series)	9 (12V/7Ah)UP1270-Unipower

TABLE III
Parameters of UPS AC/DC Converter

Boost Inductor	$L_b = 330\mu H$
DC Link Capacitors	$C1 = C2 = 3000\mu F$
Diodes D_1, D_2, D_3, D_4 and D_5	HFA25TB60
Switches S_1 and S_2	APT40GT60BR

TABLE IV
Parameters of UPS Inverters

Filter Inductors	$L_{o1} = L_{o2} = 280\mu H$
Filter Capacitors	$C_{o1} = C_{o2} = 60\mu F$
Switches S_3, S_4, S_5 and S_6 with Co-pack Diodes D_6, D_7, D_8 and D_9	IRGP35B60PD

TABLE V
Parameters of Non-Dissipative Snubber Circuit

Resonant Inductors	$L_{a1} = L_{a2} = 0.9\mu H$
Polypropylene Film Capacitors	$C_{a1} = C_{a2} = 47nF$ $C_{S1} = C_{S2} = 680nF$
Diodes D_{a1}, D_{a2}, D_{a3}, D_{a4}, D_{a5} and D_{a6}	MUR860

The experimental results consist of relevant voltage and current waveforms, and also curves that demonstrate the performance of the proposed UPS.

A. Waveforms and curves for the On-line Mode Operation

The on-line mode operation experimental results were realized with two different types of load. The results shown

in Figs. 7-11 were obtained by connecting a pure resistive load in each type of load connection accordingly to the desired output rated voltage (110Vac or 220Vac). The results shown in Figs. 12-16 were obtained when the inverters were supplying non-linear loads with crest factor of 3 and power factor of 0.65. The non-linear load used for the tests complies with the requirements of IEC62040-3.

The input voltage and the input current are shown in Figs. 7 and 12, respectively where a high power factor with low THD was obtained. For the UPS operation with non-linear loads connected at the inverters outputs, the input current THD was measured and compared to the IEC61000-3-2 standard. Fig. 13 indicates that the proposed system complies with IEC61000-3-2 standard.

The DC link capacitor voltages are shown in Figs. 8 and 14. The UPS control maintains balanced voltages in upper and lower DC link capacitors even if the inverter type of load is modified. The output voltages and currents are shown in Figs. 9, 10, 15 and 16, where it can be seen that a high quality sinusoidal voltage waveform is supplied by the inverter, independently of the characteristic of the connected load. Figs. 9 and 15 show the waveforms for full load operation at each output of the inverters, resulting in an 110V rms supply and in Figs. 10 and 16 is shown the condition for full load in both outputs, resulting in a 220V rms supply as shown in the Fig. 3. Also in the Fig. 15, the harmonic content measured of the output V_{O1} voltage was 0.53%, while the current was 119.25%. In the Fig. 16, the harmonic content

measured of the output V_{O12} voltage was 0.59%, while the current was 132.86%.

The UPS efficiency and power factor versus output power for linear load characteristic are shown in Fig. 11, where indicated voltage (110V or 220V) refers to the output types of connection. According to the experimental results in the on-line mode, the UPS proposed achieved a high efficiency even for high frequency switching operation of both converters. Compared with the systems shown in Figs. 1 and 2, that presents an efficiency of 88.8% and 87.7%, for the on-line mode respectively, this system achieved an almost equal performance considering its cost-benefit and higher commutation frequency of the converters.

B. Waveforms and curves for the Battery Mode Operation

The experimental results for the battery powered mode were carried out only for the non-linear load connected at the outputs, excepting the characteristic shown in Fig. 20 that was obtained with resistive load. The battery set voltage was adjusted around 108V, which represents the nominal voltage during intermediate test conditions.

The characteristics of the non-linear load were the same as used in on-line mode operation. Fig. 17 shows the voltage and current in the battery bank for the loads connected at the 110Vac outputs and loads connected at the 220Vac output. As shown in Fig. 17, by using the average current mode control a continuous DC current with a low ripple has been drawn from the battery set, blocking the pulsed current
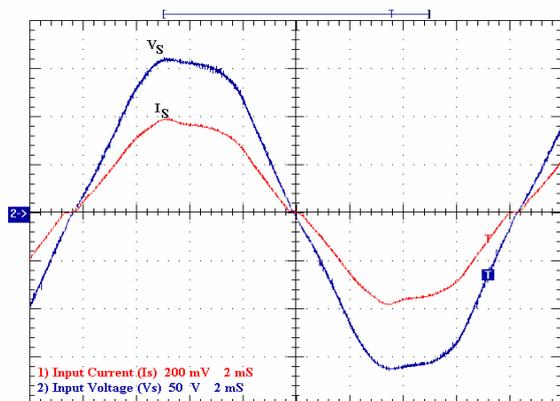
Fig. 7. Input voltage V_S and input current I_S (50V/div.; 20 A/div.; 2ms/div.)
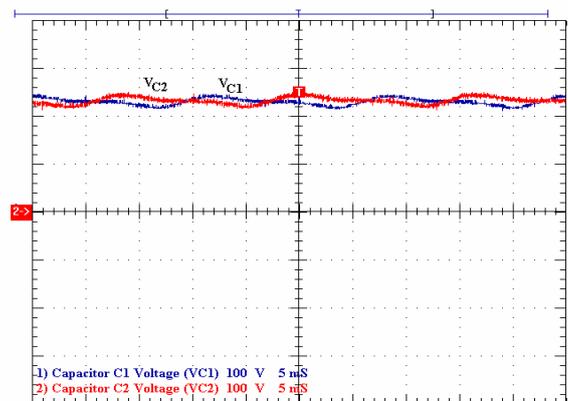
Fig. 8. DC link capacitors voltage (V_{C1}, V_{C2}) (100V/div.; 5ms/div.)
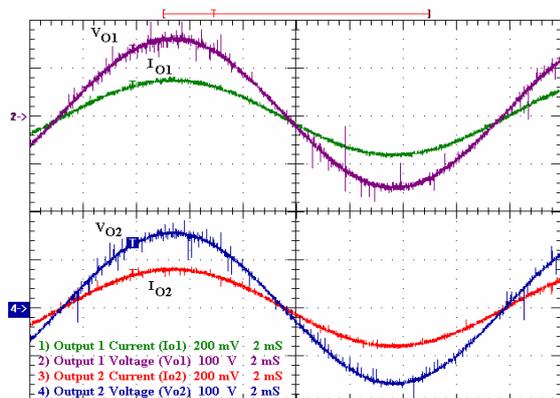
Fig. 9. Outputs voltages and currents for 110V load (100V/div.; 20A/div.; 2ms/div.)
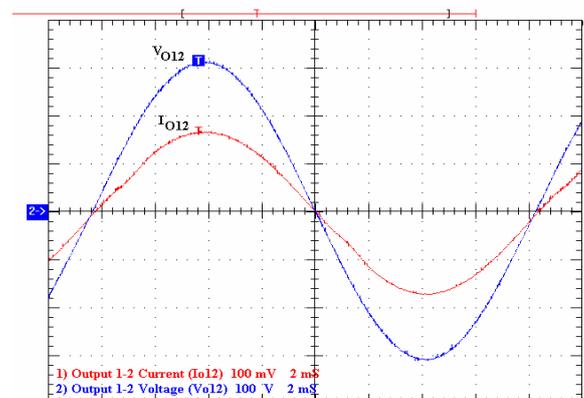
Fig. 10. Output voltage and current for 220V load (100V/div.; 10A/div.; 2ms/div.)

required by the inverters operation. Thus enhancing the reliability and life of the battery set.

The output voltages and currents are shown in Figs. 18 and 19. As in the on-line operation mode, inverters operated with the same performance. The efficiency curve for this operation mode as function of output power for the two output types of connection (110V or 220V) can be seen in Fig. 20. Most of the non-isolated UPS topologies proposed in the literature do not show their efficiency curves while the UPS is operating in this mode. Thus, compared only with Fig. 1, which presents in literature an efficiency of 86%

during battery powered mode, the topology here proposed achieved good efficiency, and this efficiency could be even improved if IGBTs of the AC/DC converter were replaced for ones with lower conduction losses. If were available discrete IGBTs with symmetric block capability, the number of diodes of this structure could be minimized, lowering the conduction losses in on-line mode and mainly in battery powered mode.

A picture of the developed prototype is shown in the Fig. 21, where it can be seen both conversion stages and the control board.

Fig. 11. Measured efficiency and input power factor of the UPS as function of output power.
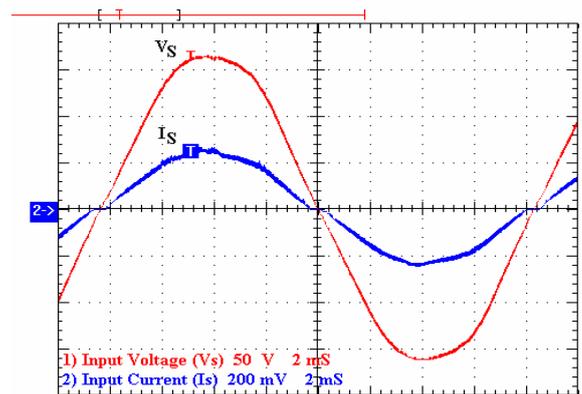
Fig. 12. Input voltage V_S and input current I_S (50V/div.; 20 A/div.; 2ms/div.)
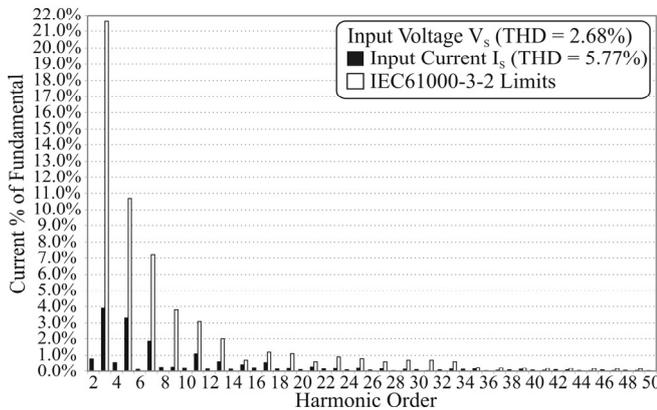
Fig. 13. Harmonic contents of I_S (Fig. 12) compared to the standard IEC61000-3-2.
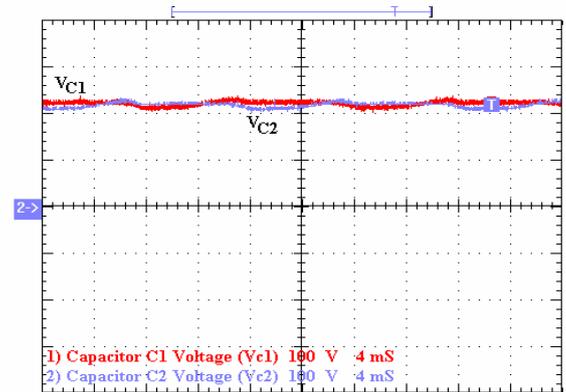
Fig. 14. DC link capacitors voltage (V_{C1}, V_{C2}) (100V/div.; 4ms/div.)
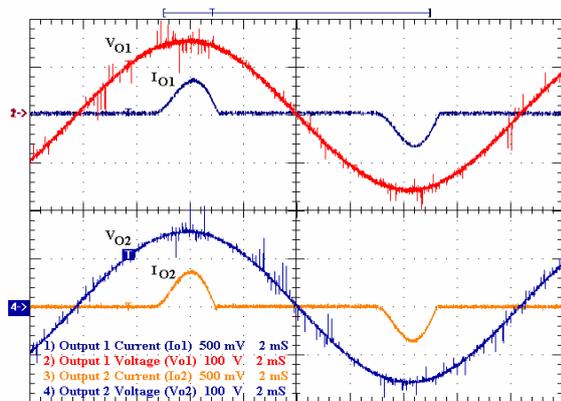
Fig. 15. Outputs voltages and currents for 110V load (100V/div.; 50A/div.; 2ms/div.)
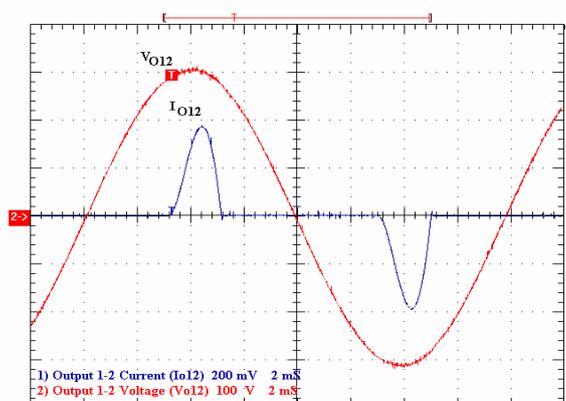
Fig. 16. Output voltage and current for 220V load (100V/div.; 20A/div.; 2ms/div.)
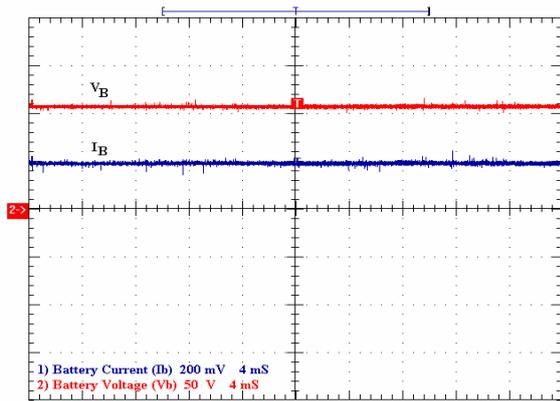
Fig. 17. Battery bank voltage V_B and current I_B (50V/div.; 20 A/div.; 4ms/div.)
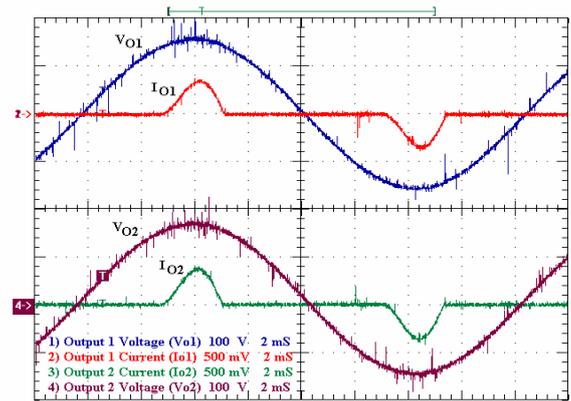
Fig. 18. Outputs voltages and currents for 110V load (100V/div.; 50A/div.; 2ms/div.)
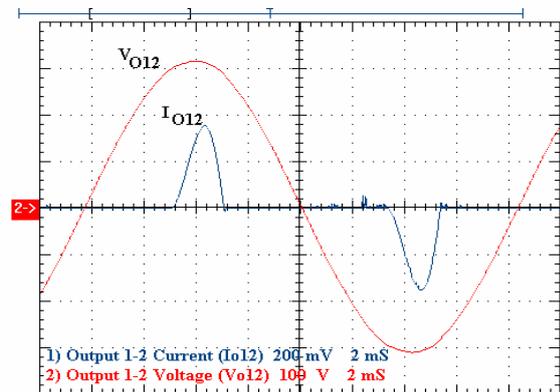
Fig. 19. Output voltage and current for 220V load (100V/div.; 20A/div.; 2ms/div.)
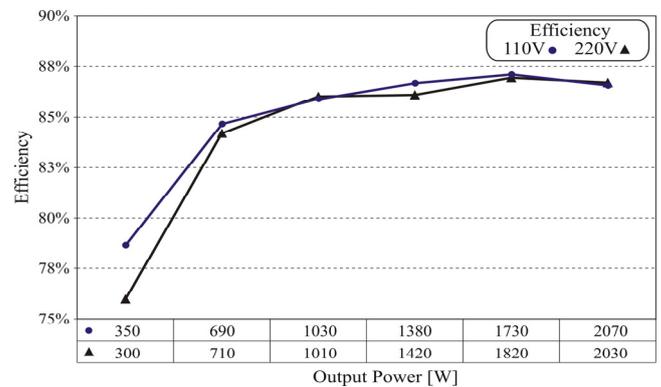
Fig. 20. Measured efficiency in battery powered mode as function of output power.
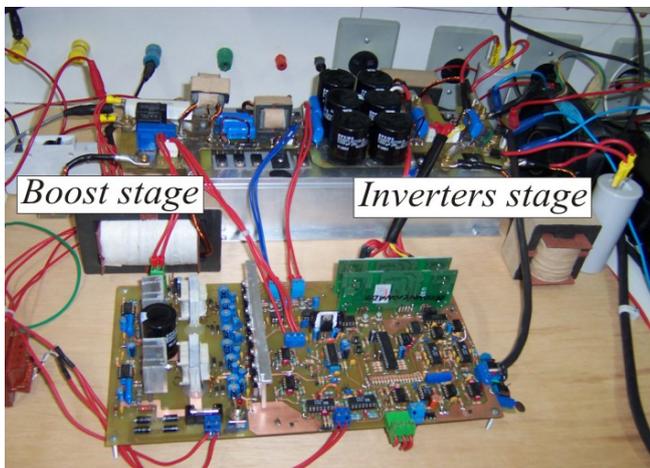
Fig. 21. Picture of the proposed UPS system.

V. CONCLUSION

This paper has proposed a non-isolated single phase 110V/220V input output voltage ratings UPS with a configuration that overcomes the problem associated with voltage doubler topologies when supplied by 220Vac of the mains.

Other advantage of the proposed topology is the possibility of supplying two different voltage ratings at the UPS output, without reducing system overall efficiency and reability. No isolating transformer is required to realize bypass operation, even if the voltage rating of the load is different from the mains voltage.

A passive non-dissipative snubber circuit was used to improve three level rectifier efficiency, while operation in both on-line and battery modes, reducing di/dt of reverse recovery mechanism in boost diodes and high current peak through the switches. Experimental results were presented to verify the performance of the proposed UPS system. This system performance could be enhanced if discrete IGBTs with lower conduction losses and symmetric block capability were available. Thus, the number of diodes of this structure also could be minimized.

The major problems of this structure are the quantity of static switches and diodes, increasing the cost and reliability. If were done a good project, the static switches could be electromagnetic relays or contactors.

Therefore, based on experimental results and compared with others topologies proposed in literature, it is possible to conclude that topology here proposed is very efficiency and attractive for the computer, telecommunications industry and others applications.

ACKNOWLEDGEMENT

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BIOGRAPHIES

Carlos Gustavo Castelo Branco was born in Fortaleza-CE, Brazil. He received the B.Sc. and M.Sc. degrees in Electrical Engineering from Federal University of Ceará, Brazil, in 2002 and 2005, respectively. Currently, he is Professor of the Federal Center of Technological Education of Piauí, Brazil. His research interests UPS systems, soft-switching techniques and converters for renewable energy sources. He is member of the Brazilian Society of Power Electronics (SOBRAEP) and the Institute of Electrical and Electronics Engineers (IEEE).

Cícero Marcos Tavares Cruz was born in Crato-CE, Brazil. He received the B.Sc. in Electrical Engineering from the Federal University of Ceará in 1990, and its M.Sc. and Dr.Eng. degrees in Electrical Engineering from Federal University of Santa Catarina, Brazil, in 1993 and 2002, respectively. Currently, he is Professor of the Department of Electrical Engineering of the Federal University of Ceará, Brazil. His research interests include Power Electronics and its application to renewable energy. He is member of the Brazilian Society of Power Electronics (SOBRAEP).

René Pastor Torrico-Bascopé was was born in Cochabamba, Bolivia. He received the B.Eng. degree in Electrical Engineering from San Simón University of Cochabamba, Bolivia, in 1992, and its M.Eng. and Dr.Eng. degrees in Electrical Engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1994 and 2000, respectively. Currently, he is Professor of the Department of Electrical Engineering of the Federal University of Ceará, Brazil. His main research interests include power supplies, power factor correction techniques, UPS systems, and alternative energy systems.

Fernando Luiz Marcelo Antunes was born in Cascavel-CE, Brazil. In 1978 he received the B.Sc. in Electrical Engineering from the Federal University of Ceará. In 1980 he received the M.Sc. degree from the University of São Paulo, Brazil, and in 1991 the PhD degree from Loughborough University of Technology, UK. He is a senior lecturer at Federal University of Ceará, Brazil, teaching Power Electronics and Electric Machines at graduate and undergraduate levels, and doing research in Power Electronics and its application to renewable energy. He is member of the Brazilian Society of Power Electronics (SOBRAEP) and the Institute of Electrical and Electronics Engineers (IEEE).