www.ietdl.org

Published in IET Power Electronics
Received on 8th April 2014
Revised on 1st July 2014
Accepted on 13th July 2014
doi: 10.1049/iet-pel.2014.0275

ISSN 1755-4535

Soft switching high-voltage gain dc–dc interleaved boost converter

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Abstract: This study presents the qualitative and quantitative analyses, design procedure and experimental results on a soft switching cell applied to a high-voltage gain interleaved boost converter. An active snubber cell is proposed as a possible solution for the increase of efficiency in a hard switching topology, where switching losses are drastically minimised. The main advantages of the introduced circuit are the common source terminal to all switches; zero-voltage switching of the main switches; zero current switching of the auxiliary switches; low-voltage stress across the switches; balanced voltage across the output capacitors; the presence of a magnetic coupling cell, which allows the gain to be significantly increased; and the magnetic components that are designed for twice the switching frequency. A prototype rated at 500 W is implemented and evaluated, where relevant issues are discussed to validate the theoretical assumptions.

1 Introduction

Several types of applications such as uninterruptible power systems and adjustable-speed drives often demand the low dc voltage from batteries, photovoltaic panels, fuel cells and small wind turbines to be stepped up. Typical low voltages range from 12 to 125 V and must be increased to 300 or 440 V so that a dc bus is obtained to supply a dc–ac stage [1].

Since high-voltage gain is a mandatory characteristic in several applications, it has led to the development of several novel converter topologies. Typically high-frequency isolated converters can play the whole of voltage step-up by adjusting the proper turns ratio, although the transformer is responsible for processing the total rated power, with consequent increase of size, weight and volume and reduction of efficiency [2]. Within this context, non-isolated dc–dc converters with high-voltage gain have been highlighted as an alternative solution in distinct applications.

It is worth to mention that the conventional boost converter is not adequate in such cases because the high output voltage demands high values for the duty cycle, which on the other hand causes the main switch to remain turned on for long time intervals in the switching period. Since the current although the diode is high, serious drawbacks concerning the reverse recovery phenomenon exist. Several approaches based on the boost converter have been proposed in the literature and some important topologies will be analysed and discussed as follows.

The connection of several boost converters in cascade would be a possible solution for voltage step-up, even though reduced efficiency is a serious drawback in this case [3]. Besides, multiple sets including active switches, magnetics and controllers imply increased cost and complexity added to the control circuit because of the high-order dynamics [4].

One of the first works concerned with non-isolated converters with large conversion ratios was proposed in [5], where multiple stages are associated in parallel to obtain high-voltage step-up converters. Thus it is possible to derive quadratic or even cubic converters, which have extensively studied in the literature through several topological modifications [6–8]. However, the use of multiple controlled switches, diodes and inductors may lead to high component count, making the proposed approach not adequate to achieve very large ratios that are typically obtained with the use of transformers.

Since the concept of the three-state switching cell (3SSC) was proposed firstly in [9], some dc–dc converter topologies with high-voltage gain characteristic have been proposed. A novel family of dc–dc converters using the 3SSC and voltage multiplier cells (VMCs) were introduced in [10], while significant advances have been achieved in terms of reduced voltage stress across the main switches, reduced input ripple current, minimisation of size, weight and volume associated to magnetics, reduced switching losses and high efficiency over the entire load range. However, the reduced useful life of series capacitors and

high component count can be pointed out as drawbacks. The topology in [11] corresponds to a boost converter using the 3SSC and a secondary winding, where the claimed advantages associated to the 3SSC are obtained [10]. Besides, for a given duty cycle, the static gain can be changed by properly adjusting the turns ratio without increasing the voltage stress for the active switches, which are less than half of the output voltage. In this structure, part of the input power is directly transferred to the load without flowing through the active switches, thus implying reduced conduction losses. Unfortunately, this converter does not work properly when the duty cycle is lower than 0.5 because of magnetic induction issues.

An extensive review on non-isolated boost converters is presented in [12], where the use of coupled inductors to achieve high-voltage gain is analysed, since they can act as a transformer that allows increasing the static gain in dc/dc converters. Numerous topologies have been introduced so far, for example, the dc–dc converter using a voltage doubler cell with reduced voltage stress across the main switch [13]. A bidirectional buck/boost converter is also studied in [14], where a passive clamp circuit is employed to minimise the voltage stress regarding the active switches. In both structures, the main drawback lies in high component count and complexity if compared with other simpler approaches existent in the literature. An interesting structure has been analysed in [15], which deserves some attention because of low component count. For instance, considering that the input voltage is 17.4 V and must be stepped up to 311 V, the maximum voltage across diode D_1 becomes very high, that is, about 800 V [15]. This may lead to the use of high-cost diodes that inherently present high forward voltage drop and also low switching speed.

Interleaving is a typical solution in high-power high-current applications, with consequent improvement of performance and reduction of size, weight and volume of magnetics [16, 17], and some approaches regarding the achievement of high-voltage gain have also been introduced. For instance, the converter studied in [18] employs two boost converters coupled through an autotransformer with unity turns ratio and opposite polarity so that the current is equally shared between the switches. Besides, voltage doubler characteristic is achieved. Even though the current stress through the switches is reduced, the respective voltage stress is less than or equal to half the total output voltage. Isolated drive circuitry must also be employed in this case. Other topologies using the interleaving technique are proposed in [19], where VMCs are adopted to provide high-voltage gain and reduced voltage stress across the semiconductor elements. In this case, interleaving allows the operation of the multiplier stages with reduction of the current stress through the devices. Besides, the size of input inductors and capacitors is drastically reduced. The voltage stress across the main switches is limited to half of the output voltage for a single multiplier stage.

A high-voltage gain interleaved boost converter is studied in [20], which operates in continuous conduction mode. The main switches are able to operate in zero current switching (ZCS) condition because of the leakage inductance, whereas discontinuous conduction mode (DCM) is maintained during the first and third operation stages. Even though the inductors operate in DCM, the input current is continuous. However, ZCS is not ensured in heavy load condition and current sharing between the inductors does not occur.

Considering high-current applications, the reduction of size, weight, cost and electromagnetic interference is of great interest and can be obtained by increasing the switching frequency at the cost of increased switching losses, which may compromise the overall efficiency. Thus soft switching using resonant techniques becomes an attractive approach, while using lossless snubbers also gives an effective solution from the viewpoint of converter efficiency and extended utilisation of power switching devices [21].

Soft switching converters have proven to be adequate for renewable energy applications because of high efficiency and reduced dimensions associated to the increase of the switching frequency. High-power density is a direct consequence in this case, as it can be stated that the overall efficiency of soft switching topologies tends to increase proportionally with the operating frequency, whereas the opposite occurs in their hard switching counterparts [22].

A soft switching interleaved boost topology with high-voltage gain is proposed in this paper, whose advantages are: low-voltage stress across the main switches, natural voltage balancing between output capacitors [23], low input current ripple and magnetic components operating at twice switching frequency. As the main drawbacks, there is the duty cycle limitation, which must be higher than 50%; and the need for soft start and initial charge of output capacitors, which is typical in topologies derived from the conventional boost converter. Firstly, the active snubber and its association to the original hard switching topology are presented. The operating stages that define the topology behaviour is also carried out, so that it is possible to derive the design procedure that allows obtaining the power stage components, that is, inductors, capacitors, switches and diodes. Finally, an experimental prototype is implemented so that it is possible to demonstrate that there is considerable increase of efficiency when compared with the hard switching converter, thus validating the theoretical assumptions.

2 Proposed converter

The proposed active snubber cell is represented in Fig. 1*a*, which is associated to switches S_1 and S_2 in Fig. 1*b*. The auxiliary circuit is formed by two diodes D_{r1} and D_3, two capacitors C_{r1} and C_{r2}, one inductor L_{r1} and one auxiliary switch S_{a1}. In the resulting topology in Fig. 1*b*, all active switches present soft switching characteristic. Main switches S_1 and S_2 operate in zero-voltage switching (ZVS) condition, whereas auxiliary switches S_{a1} and S_{a2} operate in ZCS condition. It is also worth to mention that inductor L_{b1} is coupled with inductor L_1, whereas inductor L_{b2} is coupled with inductor L_2 so that high-voltage gain can be achieved in Fig. 1*b*. On the other hand, resonant inductors L_{r1} and L_{r2} use individual cores.

At this point, it is also important to perform a brief comparison with some similar approaches that exist in the literature. For instance, the high-voltage gain interleaved boost converter in [24] presents soft switching by using a non-dissipative active snubber with less component count. However, the gain static of the resulting structure is less than that of the converter proposed in this paper. A boost-derived structure is also proposed in [25] to achieve high-voltage gain with coupled inductors, at the cost of high component count. Besides, the topology is not adequate for high-power, high-current applications, whereas

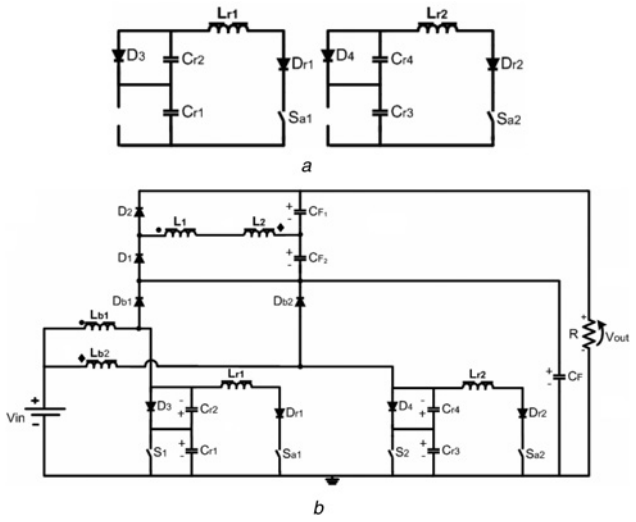

Fig. 1 *Proposed converter*

a Active snubber cell associated to switches S_1 and S_2
b Proposed soft switching interleaved boost converter

magnetics are designed for the switching frequency with resulting increase of size, weight and cost.

The qualitative analysis of the converter allows determining the expressions for the accurate design of the converter elements. The operation for one switching cycle can be divided into 14 stages. Owing to the inherent symmetry of the circuit, only the operation regarding the first active cell will be described, whereas seven stages result. The equivalent circuits are depicted in Fig. 2 and the main theoretical waveforms are represented in Fig. 3. It is also worth to mention that resonant capacitor C_{r3} is previously charged to the first stage with voltage V_{CF}.

The following parameters are also defined in Fig. 3:

$V_{g(S1)}$, $V_{g(S2)}$, $V_{g(Sa1)}$ and $V_{g(Sa1)}$ are gating signals applied to switches S_1, S_2, S_{a1} and S_{a2}; V_{Cr1}, V_{Cr2}, V_{Cr3} and V_{Cr4} are voltages across capacitors C_{r1}, C_{r2r}, C_{r3} and C_{r4}; V_{S1}, V_{S2}, V_{Sa1} and V_{Sa2} are voltages across switches S_1, S_2, S_{a1} and S_{a2}; I_{S1}, I_{S2}, I_{Sa1} and I_{Sa2} are currents through switches S_1, S_2, S_{a1} and S_{a2}; and I_{Lr1} and I_{Lr2} are currents through inductors L_{r1} and L_{r2}.

First stage [t_0, t_1] (Fig. 2a): Initially, switch S_1 and diode D_3 are on, while energy is stored in inductor L_{b1} and voltages V_{Cr1} and V_{Cr2} are null. This stage effectively begins when S_{a2} and D_{r2} are turned on in ZCS condition because of inductor L_{r2}. The current through the resonant inductor increases linearly from null to I_{Lb2}, so that D_{b2} is turned off in ZCS mode. This stage finishes when $I_{Lr2} = I_{Lb2}$.

Second stage [t_1, t_2] (Fig. 2a): This stage begins when the current through L_{r2} equals that through L_{b2}. Resonance occurs between capacitors C_{r3}, C_{r4} and inductor L_{r2}, causing C_{r3} to be discharged and C_{r4} to be charged. The stage finishes when the voltage across C_{r3} is null.

Third stage [t_2, t_3] (Fig. 2b): During this stage, resonance occurs only between C_{r4} and L_{r2}, what occurs until current ILr2 becomes null. Besides, switch S_2 is turned on in ZVS condition.

Fourth stage [t_3, t_4] (Fig. 2b): Since current I_{Lr2} is null, switch S_{a2} can be turned off in ZCS condition. Switches S_1 and S_2 remain on and energy is still stored in L_{b1} while L_{b2} is discharged. Besides, resonant capacitor C_{r4} is linearly discharged. This stage finishes when the voltage across C_{r4} is null.

Fifth stage [t_4, t_5] (Fig. 2c): When capacitor C_{r4} is discharged, diode D_4 is forward biased. The input source V_{in} also provides energy to inductors L_{b1} and L_{b2}. This stage finishes when S_1 is turned off under ZVS condition.

Sixth stage [t_5, t_6] (Fig. 2c): After switch S_1 is turned off, capacitor C_{r1} is charged by current I_{Lb1} until the voltage across it equals V_{CF}. Thus diode D_3 is reverse biased in ZVS mode, as this stage finishes when diode D_{b1} is turned on in ZVS condition.

Seventh stage [t_6, t_7] (Fig. 2d): During this stage, the current flows through D_{b1} and the energy stored in L_{b1} is transferred to capacitor C_{F2}.

3 Design procedure

3.1 Preliminary analysis and static gain

This session is concerned with the accurate design of the elements of the resonant cell shown in Fig. 1*a*. For this purpose, some parametric definitions must be defined so that the final expressions for the design of the involved elements are represented in a more simplified form.

Firstly, let us define X_a and X_b as the ratios between the resonant capacitors, which affect the static gain and the current stress across the semiconductor elements

$$C_{r2} = X_a \cdot C_{r1} \tag{1}$$

$$C_{r4} = X_b \cdot C_{r3} \tag{2}$$

Besides, the resonant capacitors can be associated so that equivalent capacitors C_{ra} and C_{rb} are given as

$$\frac{1}{C_{ra}} = \frac{1}{C_{r1}} + \frac{1}{C_{r2}} \tag{3}$$

$$\frac{1}{C_{rb}} = \frac{1}{C_{r3}} + \frac{1}{C_{r4}} \tag{4}$$

By manipulating the previous equations, it is possible to write

$$C_{r2} = (X_a + 1) \cdot C_{ra} \tag{5}$$

$$C_{r4} = (X_b + 1) \cdot C_{rb} \tag{6}$$

The angular switching frequency ω_s and angular resonance frequency ω_o are

$$\omega_s = 2 \cdot \pi \cdot f_s \tag{7}$$

$$\omega_o = 2 \cdot \pi \cdot f_o \tag{8}$$

where f_s is the switching frequency and f_o is the resonance frequency. It is worth to mention that f_o is a characteristic that defines the behaviour of the active snubber, while the following angular resonance frequencies can be defined

$$\omega_{oa} = \frac{1}{\sqrt{L_{r1} \cdot C_{ra}}} \tag{9}$$

$$\omega_{oa1} = \frac{1}{\sqrt{L_{r1} \cdot C_{r1}}} \tag{10}$$

doi: 10.1049/iet-pel.2014.0275

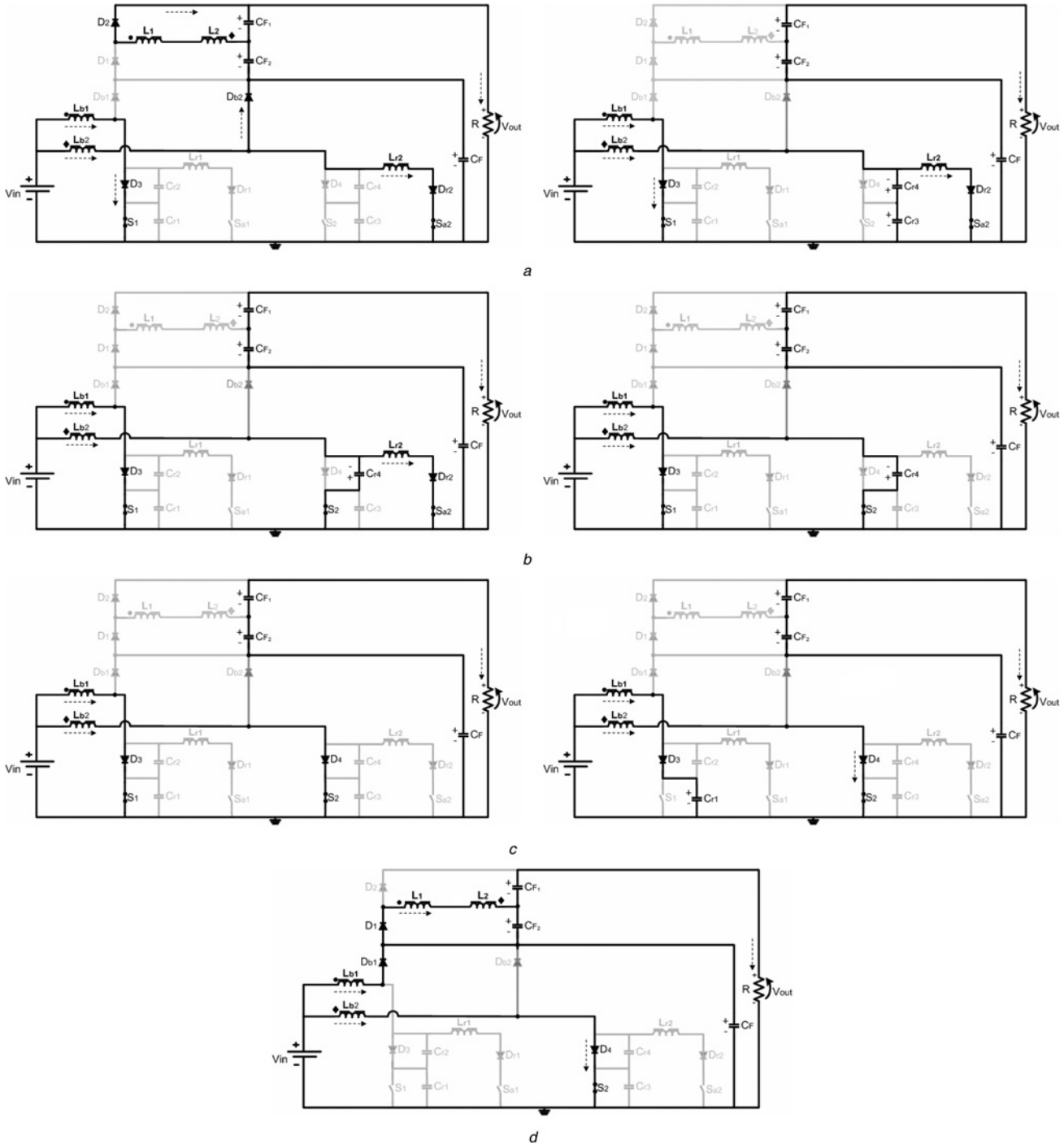

Fig. 2 *Operating stages of the proposed converter*

a First stage and second stage
b Third stage and fourth stage
c Fifth stage and sixth stage
d Seventh stage

$$\omega_{oa2} = \frac{1}{\sqrt{L_{r1} \cdot C_{r2}}} \tag{11}$$

$$\omega_{ob} = \frac{1}{\sqrt{L_{r2} \cdot C_{rb}}} \tag{12}$$

$$\omega_{ob1} = \frac{1}{\sqrt{L_{r2} \cdot C_{r3}}} \tag{13}$$

$$\omega_{ob2} = \frac{1}{\sqrt{L_{r2} \cdot C_{r4}}} \tag{14}$$

The resonant circuit impedance is a parameter which depends on the resonant inductor and the resonant capacitor of each cell and also affects the soft switching characteristic of the semiconductor elements, that is

$$Z_{oa} = \sqrt{\frac{L_{r1}}{C_{ra}}} \tag{15}$$

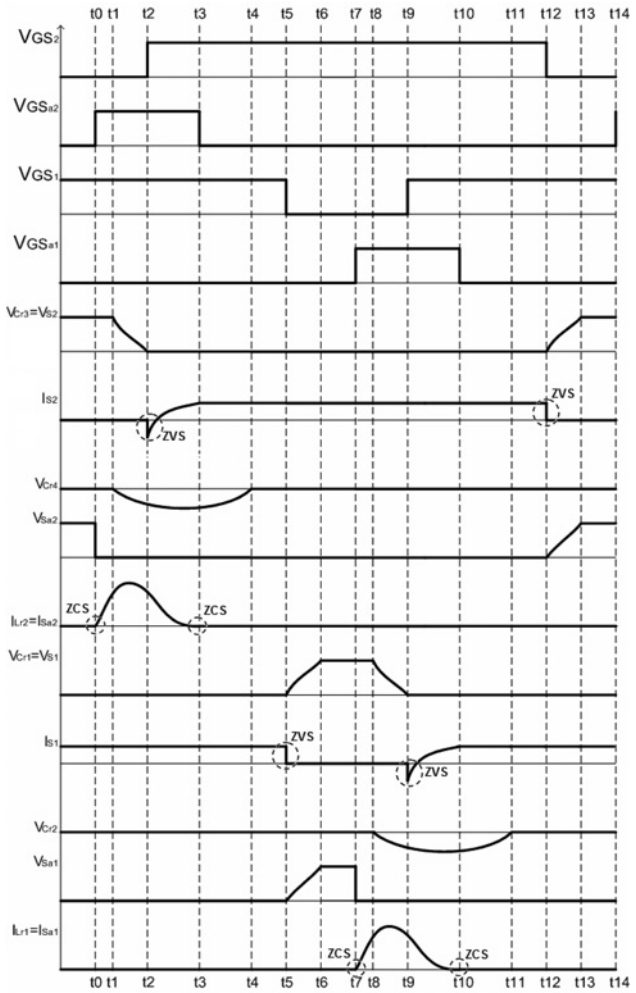

Fig. 3 *Main theoretical waveforms*

$$Z_{oa1} = \sqrt{\frac{L_{r1}}{C_{r1}}} \tag{16}$$

$$Z_{oa2} = \sqrt{\frac{L_{r1}}{C_{r2}}} \tag{17}$$

$$Z_{ob} = \sqrt{\frac{L_{r2}}{C_{rb}}} \tag{18}$$

$$Z_{ob1} = \sqrt{\frac{L_{r2}}{C_{r3}}} \tag{19}$$

$$Z_{ob2} = \sqrt{\frac{L_{r2}}{C_{r4}}} \tag{20}$$

The normalised currents involving the snubber components are represented by

$$\alpha_a = \frac{I_{in}}{V_{CF}} \cdot \sqrt{\frac{L_{r1}}{C_{ra}}} \tag{21}$$

$$\alpha_{a1} = \frac{I_{in}}{V_{CF}} \cdot \sqrt{\frac{L_{r1}}{C_{r1}}} \tag{22}$$

$$\alpha_{a2} = \frac{I_{in}}{V_{CF}} \cdot \sqrt{\frac{L_{r1}}{C_{r2}}} \tag{23}$$

$$\alpha_b = \frac{I_{in}}{V_{CF}} \cdot \sqrt{\frac{L_{r2}}{C_{rb}}} \tag{24}$$

$$\alpha_{b1} = \frac{I_{in}}{V_{CF}} \cdot \sqrt{\frac{L_{r2}}{C_{r3}}} \tag{25}$$

$$\alpha_{b2} = \frac{I_{in}}{V_{CF}} \cdot \sqrt{\frac{L_{r2}}{C_{r4}}} \tag{26}$$

where I_{in} is the input current.

The ratio between the switching frequency and the resonance frequency affects the behaviour of the snubber cell directly and must be defined as

$$K_1 = \frac{f_s}{f_o} \tag{27}$$

Parameter K corresponds to a normalised representation involving the resonant inductor and the resonant capacitor and is used to simplify both the calculations and representation of expressions, being defined as

$$K = \left(\frac{-\alpha_b}{2} \cdot \sqrt{\frac{X_b - 1}{X_b + 1}} \pm \sqrt{\frac{1}{X_b} - \frac{\alpha_b^2}{4 \cdot (X_b + 1)}} \right) \tag{28}$$

3.2 Static gains of the hard switching and soft switching converters

It is necessary to analyse the influence of the active snubber proposed in Fig. 1*a* in the static gain of the hard switching version of the converter in Fig. 1*b*. The thorough mathematical procedure that leads to the resulting static gain expression will not be discussed in detail in this paper, but it can be demonstrated

$$G = \frac{V_o}{V_{in}} = \frac{I_{in}}{I_o} = \frac{2 \cdot n + 1}{1 - D} \tag{29}$$

where n is the turns ratio of the coupled inductors in Fig. 1*b* defined as (30), V_o is the output voltage, I_o is the output current and D is the duty cycle

$$n = \sqrt{\frac{L_{b1}}{L_1}} = \sqrt{\frac{L_{b2}}{L_2}} \tag{30}$$

To determine the expression for the static gain of the soft switching converter shown in Fig. 1*b*, it is necessary to know the equivalent circuits that define the converter operation and also their respective time intervals, which are part of the switching period T_s. From analyses of Figs. 2 and Fig. 3, it is possible to determine time intervals ΔT_1,

doi: 10.1049/iet-pel.2014.0275

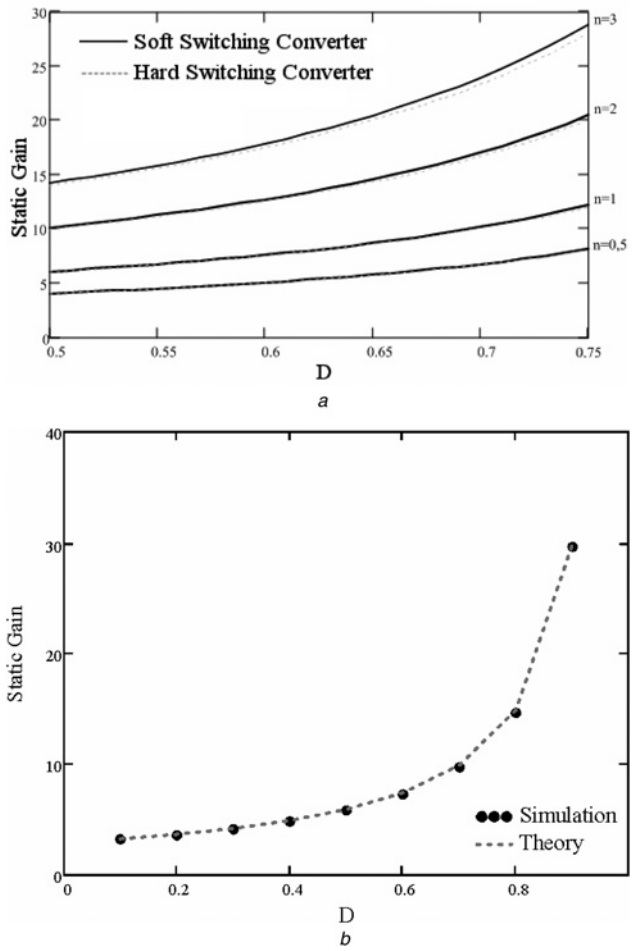

Fig. 4 *Static gain of the interleaved boost converters*

a Comparison between static gain curves of the hard and soft switching topologies

b Comparison between the theoretical curve of the static gain and the one obtained with SPICE software

…, ΔT_7 for the first seven operating stages

$$\Delta T_1 = t_1 - t_0 = \frac{\alpha_b}{\omega_{ob}} \cdot \frac{1}{2 \cdot (2 \cdot n + 1)} \tag{31}$$

$$\Delta T_2 = t_2 - t_1 = \frac{1}{\omega_{ob}} \cdot \text{acos} \cdot \left(- \frac{1}{X_b} \right) \tag{32}$$

$$\Delta T_3 = t_3 - t_2 = \frac{\sqrt{X_b + 1}}{\omega_{ob}} \cdot \text{acos}(K) \tag{33}$$

$$\Delta T_4 = t_4 - t_3 = \frac{2 \cdot (X_b + 1)}{X_b \cdot \alpha_b \cdot \omega_{ob}} \cdot \left(\sqrt{(X_b - 1) \cdot (1 - K^2)} + K \right) \tag{34}$$

$$\Delta T_5 = t_5 - t_4 = \left(- \frac{1}{2} + D \right) \cdot T_s - \Delta T_3 - \Delta T_4 \tag{35}$$

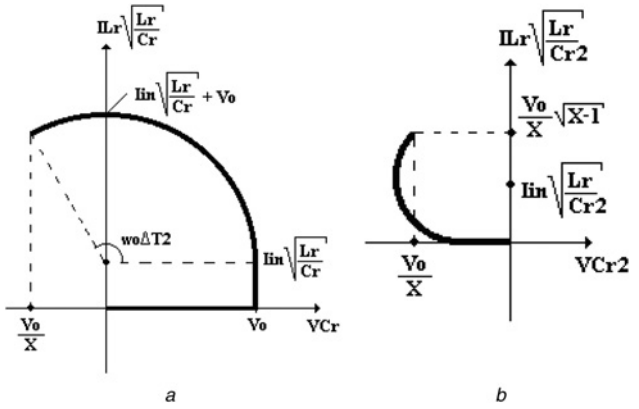

Fig. 5 *State plane of the soft switching converter*

a First state plane

b Second state plane

$$\Delta T_6 = t_6 - t_5 = \frac{2 \cdot (2 \cdot n + 1) \cdot (X_a + 1)}{X_a \cdot \alpha_a \cdot \omega_{oa}} \tag{36}$$

$$\Delta T_7 = \frac{T_s}{2} - \Delta T_1 - \Delta T_2 - \Delta T_3 - \Delta T_4 - \Delta T_5 - \Delta T_6 \tag{37}$$

It is also worth to mention that expressions for the time intervals of the remaining stages are analogous to the ones given in (31)–(37).

By manipulating the some equations, the static gain for the proposed topology shown in Fig. 1*b* can be obtained as (see (38))

It is possible to plot expressions (29) and (38) as in Fig. 4*a*. Even though the static gain expression of the soft switching converter depends on parameters that characterise the behaviour of the snubber, that is, K_1, α_b and X_b, it can be seen that the adopted cell does not influence the static gain of the hard switching topology significantly.

To validate the theoretical expression of the static gain given by (38), simulation tests were carried out in simulation program with integrated circuit emphasis (SPICE) related software using realistic models of semiconductor components provided by the application. Components D_{b1} and D_{b2} correspond to ultrafast diodes HFA25PB60 by International Rectifier; D_{r1}, D_{r2}, D_1, D_2, D_3 and D_4 are ultrafast diodes MUR460 by ON semiconductor; and the main switches and auxiliary switches are Metal oxide semiconductor field effect transistors IRFP4710 by International Rectifier. It is also worth to mention that the aforementioned semiconductor elements are the same ones used in the implementation of the experimental prototype.

The static gain plot is obtained considering $n = 1$ as defined in (30), while the duty cycle is varied from 0.1 to 0.9 in the simulation. Fig. 4*b* shows the obtained curve compared with the one given by expression (38), thus validating the theoretical assumption for the soft switching converter.

3.3 Condition for the achievement of soft switching

Considering a single snubber cell represented by Fig. 1*a*, it is possible to note that there are two distinct resonance

$$G = \frac{2 \cdot n + 1}{1 - \left\{ D + (K_1 / 2\pi) \cdot \left[\left(\alpha_b / (2 \cdot (4 \cdot n + 2)) \right) + \text{acos}\left(-(1/X_b) \right) + \left((4 \cdot n + 2)(X_b + 1) \right) / \left(X_b \cdot \alpha_b \right) \right] \right\}} \tag{38}$$

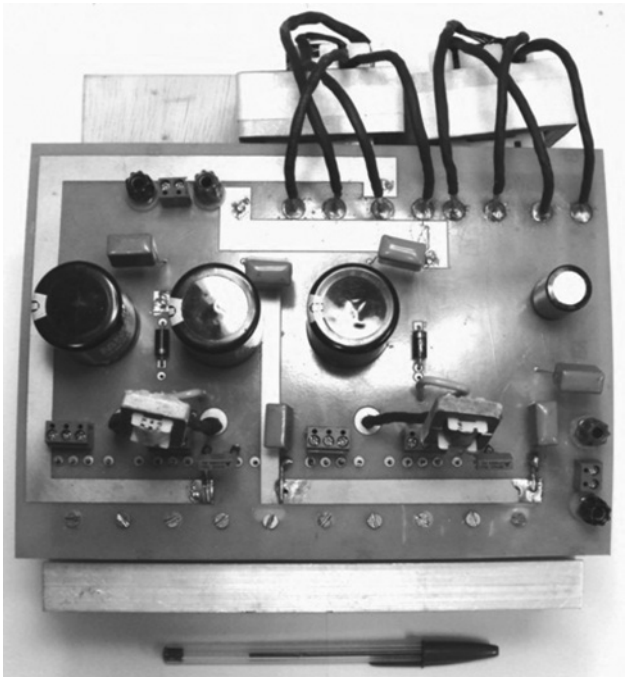

Fig. 6 *Experimental prototype*

frequencies, which are given by expressions (10) and (11), since there are two resonant capacitors and one resonant inductor. The state plane of the converter can then be divided into two plots, as shown in Fig. 5.

From the analysis of Fig. 5*a*, the following inequality can be obtained

$$X_b \geq 1 \tag{39}$$

Analogously from Fig. 5*b*, it is possible to obtain the following expression

$$X_b \leq \frac{1}{4 \cdot \alpha_{b2}^2} + 1 \tag{40}$$

It is then possible to state that the restrictions given in (39) and (40) must be obeyed so that the soft switching characteristic of the snubber cell is maintained.

3.4 Stresses regarding the semiconductor elements

The addition of the soft switching cell to the power converter involves the determination of the current and voltage stresses regarding the semiconductor elements. From the operating stages and theoretical waveforms, it is possible to properly design the diodes and switches used in the converter shown in Fig. 1*b*.

Table 1 Design specifications for the step-up converters

Parameters	Specifications
rated input voltage	$V_i = 28$ V
output power	$P_o = 500$ W
output voltage	$V_o = 180$ V
switching frequency	$f_s = 50$ kHz
estimated theoretical efficiency	$\eta = 90\%$
Designed elements	
inductors L_1, L_2, L_{b1}, L_{b2}	$L_1 = L_2 = L_{b1} = L_{b2} = 220$ μH, core NEE 65/33/26 by Thornton, 20 turns, 6 × Amerícan wire gauge (AWG) 19
resonant capacitors	$C_{r1} = C_{r3} = 27$ nF, $C_{r2} = C_{r4} = 100$ nF
resonant inductors	$L_{r1} = L_{r2} = 0.5$ μH, core NEE 20/10/5 by Thornton, 2 turns, 12 × AWG 22
capacitors C_{F1}, C_{F2}, C_F	$C_{F1} = C_{F2} = C_F = 680$ μF/250 V
diodes D_{b1}, D_{b2}	HFA25PB60
diodes D_{r1}, D_{r2}, D_1, D_2, D_3, D_4	MUR460
switches S_1, S_2, S_{a1}, S_{a2}	IRFP4710

The normalised average current, normalised root mean square (rms) current, normalised maximum current and maximum voltage regarding diode D_{b2} are given by expressions (41)–(45), respectively. It can be seen that the current stresses depend on parameters that define the behaviour of the snubber, for example,. expressions (2) and (24) (see (41 and 42))

$$\frac{I_{Db2(\max)}}{I_{\text{in}}} = \frac{1}{2 \cdot (2 \cdot n + 1)} \tag{43}$$

$$V_{Db2(\max)} = V_{\text{CF}} + V_{\text{Cr4}} \tag{44}$$

The normalised average current, normalised rms current, normalised maximum current and maximum voltage regarding auxiliary switch S_{a2} and auxiliary diode D_{r2} are given by expressions (45)–(48), respectively (see (45 and 46 at the bottom of the next page))

$$\frac{I_{Sa2(\max)}}{I_{\text{in}}} = \frac{\alpha_b + 2}{2 \cdot \alpha_b} \tag{47}$$

$$V_{Sa2(\max)} = V_{\text{CF}} \tag{48}$$

The normalised average current, normalised rms current, normalised maximum current and maximum voltage regarding main switch S_2 are given by expressions (49)–

$$\frac{I_{Db2(\text{avg})}}{I_{\text{in}}} = \frac{1}{(4 \cdot n + 2)} \left\{ 1 - D - \frac{K_1}{2 \cdot \pi} \cdot \left[\frac{\alpha_b}{2 \cdot (4 \cdot n + 2)} + \text{acos}\left(\frac{-1}{X_b}\right) + \frac{(4 \cdot n + 2) \cdot (X_b + 1)}{X_b \cdot \alpha_b} \right] \right\} \tag{41}$$

$$\frac{I_{Db2(\text{rms})}}{I_{\text{in}}} = \left\{ \frac{1}{(4 \cdot n + 2)} \cdot \left\{ 1 - D - \frac{K_1}{2 \cdot \pi} \cdot \left[\frac{\alpha_b}{(4 \cdot n + 2)} + \text{acos}\left(-\frac{1}{X_b}\right) + \frac{(4 \cdot n + 2) \cdot (X_b + 1)}{X_b \cdot \alpha_b} - \frac{\alpha_b}{3 \cdot (4 \cdot n + 2)^2} \right] \right\} \right\}^{\frac{1}{2}} \tag{42}$$

$$\frac{I_{Sa2(\text{avg})}}{I_{\text{in}}} = \frac{K_1}{2 \cdot \pi} \left\{ \frac{\alpha_b}{2} \cdot \frac{1}{[2 \cdot (2 \cdot n + 1)]^2} + \frac{1}{2} \cdot \arccos\left(-\frac{1}{X_b}\right) + \sqrt{X_b + 1} \cdot \arccos(K) + \frac{X_b + 1}{X_b \cdot \alpha_b} \cdot \left[\sqrt{(X_b - 1) \cdot (1 - K^2)} + K \right] \right\} \tag{45}$$

doi: 10.1049/iet-pel.2014.0275

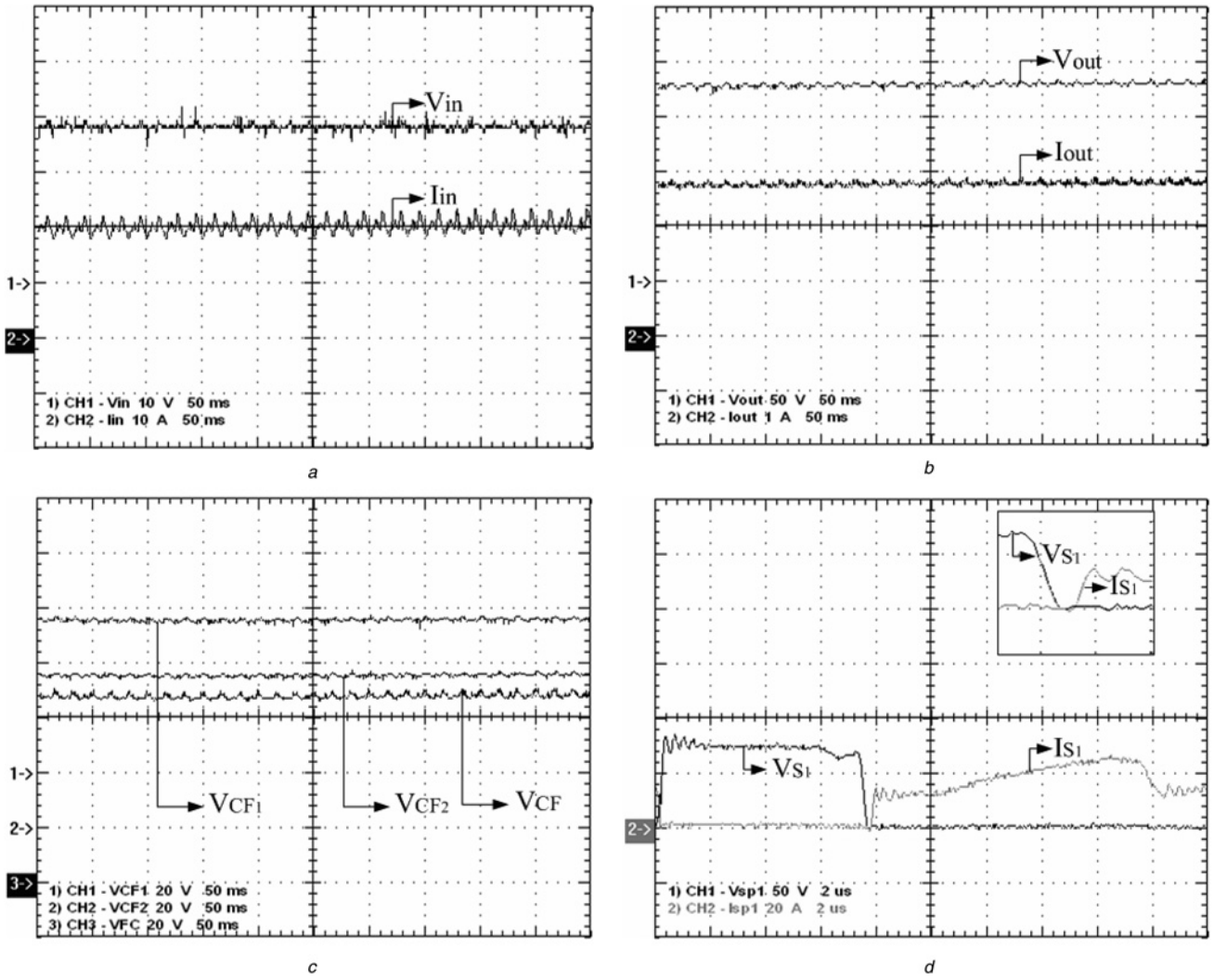

Fig. 7 *Experimental results*

a Input current and input voltage
b Output current and output voltage
c Voltages across the output capacitors
d Current and voltage waveforms of main switch S_1

(52), respectively (see (50))

$$\frac{I_{S2(\text{avg})}}{I_{in}} = -\frac{1}{2} + D + (1-D)\cdot\left(1 - \frac{1}{2\cdot(2\cdot n+1)}\right) - \frac{1}{2}\cdot\frac{K_1}{2\cdot\pi}\cdot\sqrt{X_b+1}\cdot\arccos(K) \tag{49}$$

$$\frac{I_{S2(\max)}}{I_{\text{in}}} = 1 - \frac{1}{2\cdot(2\cdot n+1)} \tag{51}$$

$$V_{S2(\max)} = V_{\text{CF}} \tag{52}$$

The normalised average current, normalised rms current, normalised maximum current and maximum voltage

$$\frac{I_{Sa2(\text{rms})}}{I_{\text{in}}} = \left\{\frac{K_1}{2\cdot\pi}\cdot\left\{\frac{1}{\left[2\cdot(2\cdot n+1)\right]^3}\cdot\frac{\alpha_b}{3} + \frac{1}{4}\cdot\text{acos}\left(-\frac{1}{X_b}\right) + \frac{1}{\alpha_b}\cdot\left(\frac{X_b+1}{X_b}\right) + \frac{1}{2\cdot\alpha_b^2}\cdot\left[\text{acos}\left(-\frac{1}{X_b}\right) + \sqrt{\frac{X_b^2+1}{X_b^4}}\right] + \frac{1}{4}\cdot\sqrt{X_b+1}\cdot\text{acos}(K) + \frac{1}{\alpha_b}\cdot\frac{(X_b+1)}{X_b}\cdot\left[\sqrt{(X_b+1)\cdot(1-K^2)} + K - 1\right] + \frac{\sqrt{X_b+1}}{\alpha_b^2}\cdot\frac{(X_b+1)}{X_b^2}\cdot\left[\frac{X_b}{2}\left(\arccos(K) + \sqrt{1-K^2}\cdot K\right) - \sqrt{X_b-1}\cdot\sqrt{1-K^2}\right]\right\}\right\}^{1/2} \tag{46}$$

$$\frac{I_{S2(\text{rms})}}{I_{\text{in}}} = \left[-\frac{1}{2} + D + (1-D)\cdot\left(1 - \frac{1}{2\cdot(2\cdot n+1)}\right) - \frac{1}{2}\cdot\frac{K_1}{2\cdot\pi}\cdot\sqrt{X_b+1}\cdot\arccos(K)\right]^{1/2} \tag{50}$$

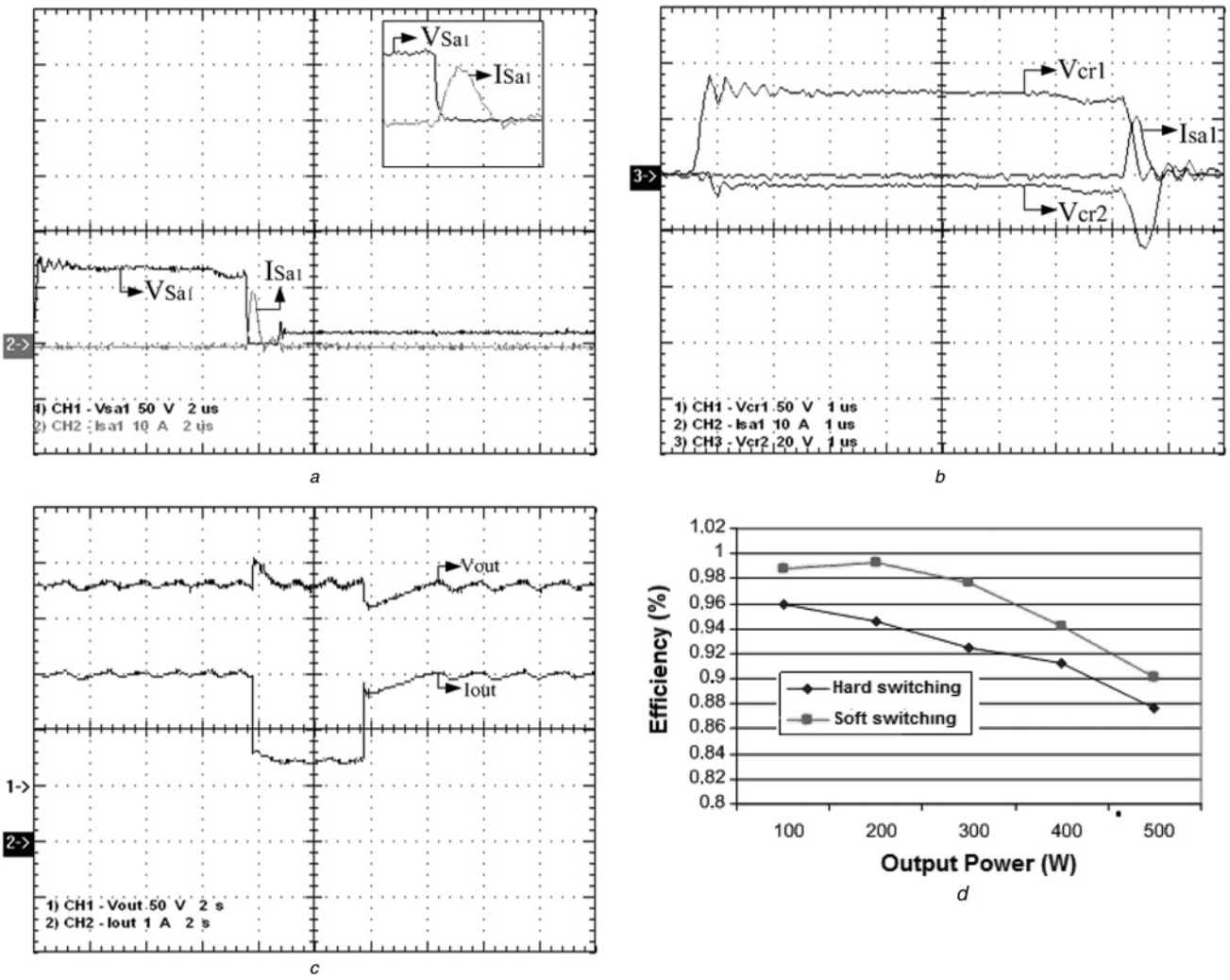

Fig. 8 *Experimental results*

a Current and voltage waveforms of auxiliary switch S_{a1}
b Voltages across capacitors C_{r1} and C_{r2} and current through auxiliary switch S_{a1}
c Output voltage and output current during a load step
d Efficiency as a function of the output power

regarding auxiliary diode D_4 are given by expressions (53)–(56), respectively (see (53 and 54))

$$\frac{I_{D4(\max)}}{I_{\text{in}}} = 1 - \frac{1}{2 \cdot (2 \cdot n + 1)} \tag{55}$$

$$V_{D4(\max)} = V_{Cr4} \tag{56}$$

4 Experimental results

To validate the theoretical assumptions, the experimental prototype shown in Fig. 6 was designed and evaluated, whose specifications are given in Table 1. Some waveforms obtained at rated load condition are presented and discussed as follows.

Fig. 7*a* presents the input current and input voltage waveforms, whose average values are rated at 20 A and 28

$$\frac{I_{D4(\text{avg})}}{I_{\text{in}}} = -\frac{1}{2} + D + (1-D) \cdot \left(1 - \frac{1}{2 \cdot (2 \cdot n + 1)}\right) + \frac{K_1}{2 \cdot \pi} \cdot \left(-\frac{1}{2} \cdot \sqrt{X_b + 1} \cdot \arccos(K) - \frac{(X_b + 1)}{X_b \cdot \alpha_b} \cdot \left[\sqrt{(X_b - 1) \cdot (1 - K)} + K - 1\right]\right) \tag{53}$$

$$\frac{I_{D4(\text{rms})}}{I_{\text{in}}} = \left[-\frac{1}{2} + D + (1-D) \cdot \left(1 - \frac{1}{2 \cdot (2 \cdot n + 1)}\right) + \frac{K_1}{2 \cdot \pi} \cdot \left(-\frac{1}{2} \cdot \sqrt{X_b + 1} \cdot \text{acos}(K) - \frac{(X_b + 1)}{X_b \cdot \alpha_b} \cdot \left[\sqrt{(X_b - 1) \cdot (1 - K)} + K - 1\right]\right)\right]^{1/2} \tag{54}$$

doi: 10.1049/iet-pel.2014.0275

V, respectively. Besides, the average output current and output voltage are shown in Fig. 7*b*, which are about 2.78 A and 180 V, respectively.

Fig. 7*c* presents the waveforms regarding the output capacitors, where it can be seen that the voltages across C_{F1} and C_{F2} are balanced, although there is a slight difference in the voltage across C_F. It occurs because V_{CF1} and V_{CF2} depend on the turns ratio and leakage inductance of the inductors, whereas V_{CF} depends only on the duty cycle.

According to Fig. 7*d*, it can be seen that ZVS turn on occurs for main switch S_1, whereas ZCS turn on is verified in the waveforms shown in Fig. 8*a* for auxiliary switch S_{a1}. Switching losses are then drastically reduced if compared with the hard switching version of the topology in Fig. 1*b*.

The waveforms regarding the resonant capacitors C_{r1} and C_{r2} and auxiliary switch S_{a1} are represented in Fig. 8*b*, which are similar to those predicted in the theoretical analysis and are analogous to those regarding capacitors C_{r1}, C_{r2} and S_{a1}.

The behaviour of the output voltage during positive and negative load steps is presented in Fig. 8*c*, where it can be seen that the converter operation is stable. It is worth to mention that the design of the control system is based on the transfer function of the output voltage to the duty cycle, which is the same as that of the classical boost converter. Therefore the detailed design procedure of the control system will not be presented in this paper.

Finally, the efficiency curves of the hard switching (without the use of the snubber cell shown in Fig. 1*a*) and soft switching topologies are shown in Fig. 8*d*, where the same operating conditions are assumed to establish a fair comparison. The efficiency of the proposed converter is significantly higher than that achieved by the original topology over the entire load range. The difference may be up to 4% when the converter is evaluated from light load to heavy load conditions.

5 Conclusions

This paper has presented the qualitative analysis, operating principle, theoretical waveforms and experimental results on an active soft switching cell applied to a high-voltage gain interleaved boost converter. It has been shown that the active switches present ZVS commutation, whereas the auxiliary switches operate under ZCS condition, thus leading to the significant reduction of switching losses.

The theoretical analysis has demonstrated that the static gain of the original topology remains practically unaffected when the snubber is added. Good voltage balance involving the output capacitors is also achieved, with a slight unbalance involving capacitors C_{F1}–C_{F2} and C_F.

The most significant advantage of the proposed converter lies in the increased efficiency if compared with the hard switching topology because of the significant reduction of switching losses. At rated load, it has been shown the efficiencies for the original converter and the soft switching one are 87.67 and 91%, respectively. Even though high component count and some complexity can be addressed to the arrangement, its application becomes interesting at high-current high-power applications where the switching frequency and power levels may become high enough to compromise the overall efficiency.

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