Electric Power Systems Research 143 (2017) 703–714

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

A new bidirectional hybrid multilevel inverter with 49-level output voltage using a single dc voltage source and reduced number of on components

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ARTICLE INFO

Article history:
Received 16 May 2016
Received in revised form 7 October 2016
Accepted 14 October 2016
Available online 4 November 2016

Keywords:
Asymmetrical multilevel inverter
Bidirectional switches
DC–AC converter bidirectional
Stage ca–ca
Multiple winding transformer

ABSTRACT

This paper proposes an isolated bidirectional asymmetrical multilevel inverter topology composed by an H-bridge (HB) inverter connected to the primary side of transformer. The transformer secondary side is composed by two windings, and each one is connected to a new cell introduced in this work. The proposed new cell is based on the conventional HB inverter, where two bidirectional switches are added to each HB leg, thus resulting in the structure referred to as CHB-2bs. The transformer can also be composed by multiple secondary winding in order to provide the necessary voltages to supply as many as CHB-2bs cells are. A 600 W laboratory prototype with dc input voltage of 48 V and an ac output voltage of 220 V, 60 Hz using a grain-oriented silicon–steel toroidal transformer operating at 300 Hz is implemented to validate the theoretical assumptions and the advantages addressed to the CHB-2bs cell.

1. Introduction

Different strategies for the integration of energy sources are becoming increasingly present nowadays, where the inclusion of renewable energy is supposed to modify the dynamic behavior of traditional one way energy flow power systems [1–6]. The ever increasing electricity generation at the consumer side and the advent of microgrids made the bidirectional power flow to play an important role [7,8]. Within this context bidirectional power converters are quite important when interconnecting storage systems, solid-state transformers (SSTs), microgrids and electric vehicles to the power grid [9–15]. All of the aforementioned fields correspond to potential applications of multilevel inverter topologies. Arrangements called asymmetrical or hybrid inverters have been presenting significant interest in generating more levels in the output voltage with fewer components [16,17].

Currently asymmetrical multilevel inverters are frequently applied in FACTS (flexible ac transmission systems) devices [18], especially for STATCOMs (Synchronous Static Compensators), electric machines drives, and renewable energy systems. Moreover, when the inverter is applied to machine drives, torque ripples are greatly reduced when compared to other topologies [19].

The main disadvantage of asymmetrical topologies compared to other aforementioned approaches lies on the required number of additional isolated voltage sources. However, it is drastically reduced when compared to symmetrical cascade topologies to provide an output voltage with the same number of levels. Solutions using a single dc voltage source have been successfully implemented with low-frequency inverters and multi-winding transformers. Besides, research for new materials and magnetic cores has shown that it is possible to process tens of kilowatts with efficiencies higher than 99.4% [20], which brings prominent advantages for the implementation of such topologies. Within this context, this paper proposes a new multilevel asymmetrical inverter topology based on the HB cell with two bidirectional switches, resulting in a base module called CHB-2bs. Several asymmetrical configurations for the proposed topology are presented, while using a suitable input voltage for the two cascaded CHB-2bs cells can provide an output voltage waveform with up to 49 levels.

A prototype with dc input voltage of 48 V and an ac output voltage of 220 V using a grain-oriented silicon–steel toroidal transformer operating at 300 Hz is implemented to validate the theoretical assumptions. It can be stated that the proposed approach increases the converter efficiency, also maintaining low total harmonic distortion of the output voltage and reducing the total number of on components when compared with the conventional multilevel converter using an ac–ac stage to produce the same number of levels of the output voltage waveform. The theoretical analysis is carried out and experimental results are discussed to

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http://dx.doi.org/10.1016/j.epsr.2016.10.041
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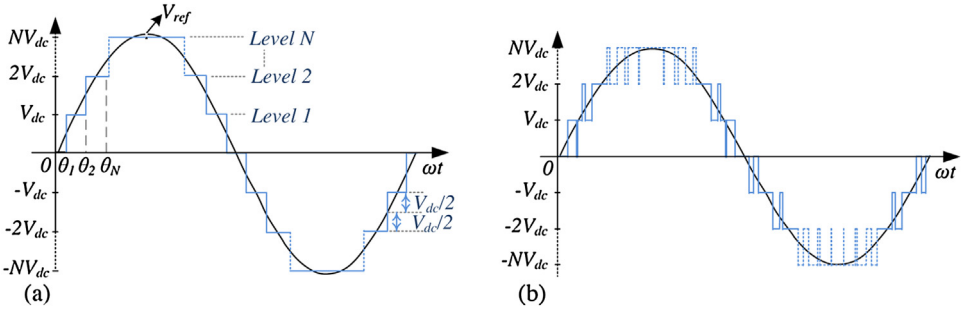

Fig. 1. *N*-level output voltage waveform during one quarter cycle: (a) fixed levels; (b) modulated levels.

evaluate the proposed converter with ac–ac stage, which does not require the use of an additional diode bridge. A study for the converter operating with n levels for the output voltage is presented, as well as relevant mathematical expressions. Finally, important issues are discussed and eventual comparison is performed with other asymmetrical topologies.

2. Features and performance of multilevel inverters

Multilevel inverters are characterized by the improved distribution of the voltages stresses across the semiconductors, thus making them suitable for a wide range of applications that involve high power and medium voltage levels [9]. In the early days of this technology [21], this aspect had direct impact on the output voltage in terms of a multilevel waveform, as shown in Fig. 1(a). However, nowadays there are multilevel inverters where the voltage stresses across the semiconductors are not equally shared, although they are able to generate the same multilevel waveform *Vo* with the advantage of reducing the number of required components. Such topologies are widely known in literature as hybrid inverters due to the use of semiconductor devices with distinct technologies e.g., integrated gate commutated thyristors (IGCTs) and insulated gate bipolar transistors (IGBTs), also called asymmetrical inverters due to employing dc voltage sources with distinct magnitudes to supply the cascaded cells [15,22–25].

The output voltage waveform in a multilevel inverter with n levels can be generated with fixed levels as in Fig. 1(a) or modulated levels as in Fig. 1(b). The operation with fixed levels is adequate for high power applications where each angle θ_N can be used to eliminate harmonics. Fig. 1(b) shows that the inverter output voltage is expressed by modulated levels, resulting from the use of pulse width modulation (PWM) strategies such as phase disposition (PD), alternative phase opposite disposition (APOD), phase opposition disposition (POD), phase shift (PS), hybrid modulation, space vector modulation (SVM), among others [9,26,27]. Usually one of the main advantages addressed to PWM is the concentration of the harmonic amplitudes around the switching frequency, which are far from the fundamental component, thus making harmonic filtering easier in terms of smaller filter elements when compared to those used in inverters operating with the same number of fixed levels n. However when operating levels with many fixed voltage levels, the harmonic content of the output voltage is drastically affected.

The inverter topology studied in this work employs staircase modulation, which produces an output voltage as shown in Fig. 1(a).

The output voltage $v_o(\omega t)$ presented in Fig. 1(a) can be expressed in terms of the Fourier series given by:

$$v_o(\omega t) = \frac{a_0}{2} + \sum_{k=1}^{\infty}(a_k \cos\ kwt + b_k\ \sin\ kwt) = \sum_{k=-\infty}^{\infty}(C_k e^{-jk\omega t}) \tag{1}$$

where a_0, a_k, and b_k are the Fourier series coefficients, and C_k is the magnitude of the k-th harmonic.

$$\begin{aligned} C_k &= \frac{1}{2\pi}\int_{-\pi}^{\pi} v_o(\omega t)e^{-jk\omega t}d\omega t \\ &= \frac{1}{2\pi}\sum_{i=1}^{N}\left[\int_{-(\pi-\theta_i)}^{-\theta_i} -V_{dc}e^{-jk\omega t}d\omega t + \int_{\theta_i}^{\pi-\theta_i} V_{dc}e^{-jk\omega t}d\omega t\right] \\ &= \frac{V_{dc}}{2\pi k}\sum_{i=1}^{N} j\left[-\left(e^{jk\theta_i}+e^{-jk\theta_i}\right)+\left(e^{jk(\pi-\theta_i)}+e^{-jk(\pi-\theta_i)}\right)\right] \\ &= \frac{V_{dc}}{2\pi k}\sum_{i=1}^{N} j\left[\cos(k(\pi-\theta_i))-\cos(k\theta_i)\right] \end{aligned} \tag{2}$$

where V_{dc} is the dc input voltage.

Since voltage $v_o(\omega t)$ has central symmetry, the dc component (term a_0) and even harmonics are null. Thus the output voltage expressed in terms of the Fourier series becomes:

$$v_o(t) = \sum_{i=1}^{N}\sum_{k=1}^{\infty}\frac{2V_{dc}}{k\pi}\left[\cos(k\theta_i)-\cos\left(k(\pi-\theta_i)\right)\right]\sin(k\omega t) \tag{3}$$

The fundamental component of the output voltage Vo_{f1} employing staircase modulation in Fig. 1(a) is:

$$Vo_{f1} = \frac{4V_{dc}}{\pi}\sum_{i=1}^{N}\cos(\theta_i) \tag{4}$$

The $(2l-1)$-th harmonic components of the output voltage are given by:

$$Vo_{h(2l-1)} = \frac{4V_{dc}}{(2l-1)\pi}\sum_{i=1}^{N}\cos\left[(2l-1)\theta_i\right] \tag{5}$$

for $l = 2, 3, 4, \ldots.$

In order to check the quality of the resulting waveform, the total harmonic distortion (THD) index given by Eq. (6) can be used. According to standard IEEE Std 519, the THD of the resulting output voltage must be lower than 5%.

$$THD = \frac{\sqrt{\sum_{l=2}^{\infty}\left[\frac{4V_{dc}}{2l-1}\sum_{i=1}^{N}\cos(2l-1)\theta_i\right]}}{\frac{4V_{dc}}{\pi}\sum_{i=1}^{N}\cos\left(\theta_i\right)} \tag{6}$$

From Eq. (4), the modulation index *mi* can be obtained to determine the output voltage amplitude considering a given number of levels N during one quarter cycle i.e.:

$$mi = \frac{Vo_{f1}\pi}{4NV_{dc}} \tag{7}$$

Expressions Eqs. (4) and (5) can be used to determine θ_i and eliminate dominant harmonics, always resulting in a system with N available transcendental equations, wherein the first equation is used to find the fundamental component as in Eq. (8). Isolating the cosine terms and assuming that the harmonic amplitudes are equal to zero i.e., $V_{h(2l-1)} = 0$, the $N-1$ harmonic components can be eliminated:

$$\begin{aligned}
&\cos(\theta_1) + \cos(\theta_2) \ldots \cos(\theta_N) = \frac{\pi V o_{f1}}{4V_{dc}} \\
&\cos(3\theta_1) + \cos(3\theta_2) \ldots \cos(3\theta_N) = 0, ** \\
&\cos(5\theta_1) + \cos(5\theta_2) \ldots \cos(5\theta_N) = 0 \\
&\vdots \quad \vdots \quad \vdots \\
&\cos(7\theta_1) + \cos(7\theta_2) \ldots \cos(7\theta_N) = 0 \\
&\vdots \quad \vdots \quad \vdots \\
&\sum_{i=1}^{N} \cos\left[(2l-1)\theta_i\right] = 0
\end{aligned} \tag{8}$$

**where $l = 2$, $l = 3p - 1$, $p = 1, 2, 3\ldots$, as this expression is only valid for single-phase inverters considering the phase voltage. The third harmonic $V_{h(3)}$ and its respective even multiples do not exist in the line voltage and thus $l \neq 3p - 1$ in Eqs. (5), (6), and (8) when applied to the line voltage.

The line voltage in three-phase systems is $\sqrt{3}$ times higher than the phase voltage and can be considered as a sum given by $v_o(t) + v_d(t)$, where $v_d(t)$ corresponds to $v_o(t)$ lagged by $\frac{1}{3f1}$.

Several approaches can be used for the solution of Eq. (8) e.g., resultant theory, Newton–Raphson, genetic algorithms, computational tools, among others based on numerical methods [28–31].

3. Proposed topology

The topology proposed in this work is shown in Fig. 2, being composed by a dc voltage source *Vin* responsible for supplying the input bus of the HB cell, which in turn imposes an ac voltage to the primary side of the multi-winding transformer operating at medium frequency. It is worth to mention that the transformer provides the desired voltage across each CHB-2bs cell.

Generic aspects of the aforementioned topology are described in Section 4.

3.1. Prominent advantages and applications of the proposed topology

The main advantage addressed to the topology when compared with other multilevel cascaded inverters lies on the drastic reduction in the number of required dc voltage sources. It needs a single one only as seen in Fig. 2.

Other features such as insulation, possibility to associate the output side in series with other inverters to generate a larger bus without short-circuit issues, operation at reduced frequency due to the use of staircase modulation, absence of electromagnetic shielding to eliminate conducted and radiated electromagnetic interference (EMI), as well as the absence of output filter elements (or use of small-sized ones) are some prominent advantages of the converter.

Another interesting aspect of this approach lies in increased robustness due to the absence of electrolytic capacitors in the cells, since such components typically present short useful life, and also the absence of complex techniques to balance the voltages across them. It is also possible to mention that the semiconductors present thermal relief due to existence of minimized stresses and operation with reduced frequency.

Considering the aforementioned aspects, it can be stated that the potential applications of the topology include standalone systems using PV modules as a primary source. Besides, it can be applied

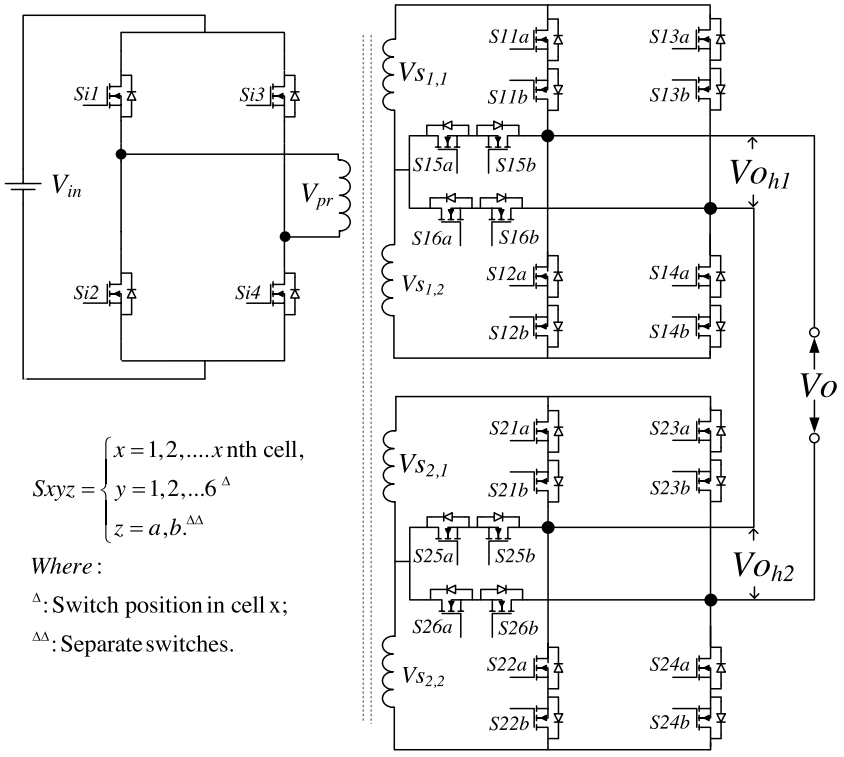

Fig. 2. Proposed topology with an intermediate ac–ac stage.

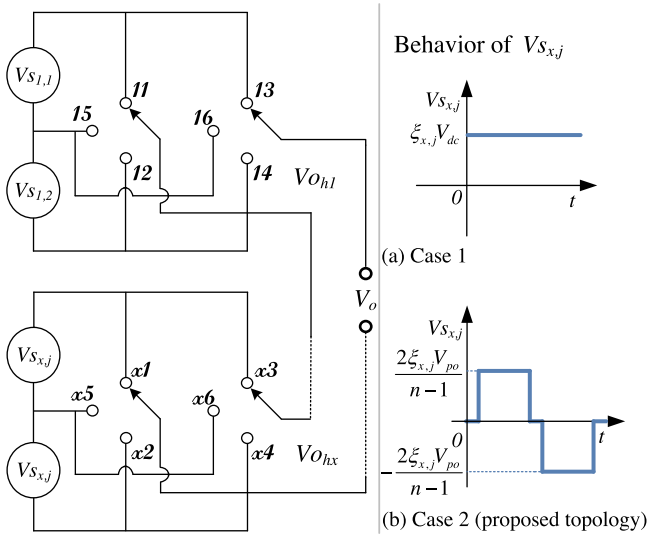

Fig. 3. Generic configuration of the proposed structure with cascaded CHB-2bs cells. (a) Operation with dc voltage sources and (b) operation with ac voltage sources. Where: V_{po} is the peak value of output voltage with n levels.

to microgrids as an interface with renewable energy sources, or as a link between the dc bus and ac systems due to the inherent bidirectional characteristic.

4. General characteristics of the topology

The cascaded CHB-2bs cells must operate with bidirectional switches for the adequate operation of the proposed topology as shown in Fig. 2.

The adopted configuration for the bidirectional switches *Sxyz* employs two antiseries-connected n-channel MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) (with common source connection), which is responsible for ensuring the path for current i_o according to the switching logic, with consequent reduction of power losses if compared with the use of low-voltage IGBTs.

The independent drive of the bidirectional switches *Sxyz* (*Sxya* or *Sxyb*) results in a modular topology, also allowing both switches Sxya and *Sxyb* to be turned on simultaneously instead of one MOSFET and one diode of a switch *Sxyz* during a given state with level *n*.

The simultaneous turn on of one switch and one diode in a given bidirectional switch *Sxyz* is avoided in this work, since it implies higher losses. This configuration is also adopted during the intervals corresponding to level transitions, while minimizing the diode on-time.

4.1. General operation modes of the topology

The association of voltage sources $Vs_{x,j}$ (where j corresponds to the position of the source in cell x i.e., $j=1$ or $j=2$) must provide equally-spaced levels with the same magnitude according to Fig. 1(a) so that the THD of the output voltage is not affected.

The restrictions imposed to the commutation when double gating signals are applied to *Sxyz* must comply with the complementarity conditions of the HB cell, as well as switches *Sx5z* and *Sx6z* must obey the restrictions imposed by Eq. (9).

$$Sx5z \leftrightarrow \overline{Sx1z} \quad , \quad \overline{Sx2z} \qquad \text{and} \qquad Sx6z \leftrightarrow \overline{Sx3z} \quad , \quad \overline{Sx4z} \tag{9}$$

where $x=1, 2, \ldots$ corresponds to the first, second, $\ldots x-$nth cell, respectively, and $z=\{a,b\}$.

Then, observing a given CHB-2bs cell in the proposed topology in Fig. 2 and also the simplified circuit in Fig. 3, it is possible to choose cases 1 and 2 using only positive values for $Vs_{x,j}$ considering $Vs_{x,2}=2Vs_{x,1}$. Seven different ideal levels result in the output voltage Vo_{hx} when using double gating signals for *Sxyz*, considering only term *Sxy* i.e.,

$$Vo_{hx}=\begin{cases} 0 \rightarrow Sx1 \text{ and } Sx3,\ Sx2 \text{ and } Sx4 \text{ or } Sx5 \text{ and } Sx6, \\ Vs_{x,1} \rightarrow Sx1 \text{ and } Sx6, \\ -Vs_{x,1} \rightarrow Sx3 \text{ and } Sx5, \\ 2Vs_{x,1} \rightarrow Sx5 \text{ and } Sx4, \\ -2Vs_{x,1} \rightarrow Sx2 \text{ and } Sx6, \\ 3Vs_{x,1} \rightarrow Sx1 \text{ and } Sx4, \\ -3Vs_{x,1} \rightarrow Sx2 \text{ and } Sx3. \end{cases} \tag{10}$$

During the transition between adjacent states as shown in Eq. (10), it is not possible to change the switches commutation according to the aforementioned configuration, since overvoltage across switches *Sxyz* may occur when supplying inductive loads, for example.

An alternative to avoid voltage spikes during the level transition has been implemented in Ref. [14], based on the application of a passive snubber to each switch *Sxyz*. However, it implies increased cost and the component count.

Due to the adopted switching configuration, an additional snubber is not used to ensure the current flow during the level transition. The configuration corresponding to turning on one switch and one diode in *Sxyz* is only used during the level transition period as $t \leq 1$ μs, so that safe operation of the power converter is ensured when inductive loads are supplied. This technique enables current i_o to flow, thus avoiding damaging voltage spikes across switches *Sxyz* due to $L\frac{di}{dt}$ effect. It is also worth to mention that the adopted driving strategy always allows one switch of *Sxyz* (*Sxya* or *Sxyb*) to remain on due to the polarity of the voltage across the primary winding *Vpr*.

Distinct combinations of switches *Sxya* and *Sxyb* and their respective diodes and the current direction i.e., $i_o>0$ or $i_o<0$ in the CHB-2bs cell represented by x can be verified in order to maintain the current flowing during a level transition.

This work uses only one intermediate state during the level transition, while the simultaneous turn on of two MOSFETs in a bidirectional switch *Sxyz* is maintained for a state with level n, thus resulting in reduced losses. Other strategies for the generation of *n* levels can be achieved by turning on one switch and one diode of the adjacent switch in *Sxyz* (*Sxya* and *Sxyb*) analogously to the implementation given in Ref. [32], even though higher losses result since the diodes are forward biased.

The weight of a voltage source $\xi_{x,j}$ in position j is $\xi_{x,j}=Vs_{x,j}/Vs_{1,1}$ for a given cell, as x is related to the weight of cell P_x, i.e., $P_x=Vs_x/Vs_{1,1}$, where Vs_x is the bus voltage across cell x i.e., $Vs_x=Vs_{x,1}+Vs_{x,2}$.

The association of cascaded cells can generate different combinations when varying parameter $\xi_{x,j}$, resulting in more equally-spaced levels in the output voltage, also using the same number of components.

This can be accomplished by a specific relationship among distinct weights P_x (normalized as function of $Vs_{1,1}$, $Pnor_x$) and related by an integer multiplicative factor as in Eq. (11).

$$Pnor_x = \{x \in \mathbb{N}^* : \left(\frac{Vs_1}{Vs_{1,1}}\right), \left(\frac{Vs_2}{Vs_{1,1}}\right), \left(\frac{Vs_3}{Vs_{1,1}}\right) \ldots \left(\frac{Vs_{x-2}}{Vs_{1,1}}\right), \left(\frac{Vs_{x-1}}{Vs_{1,1}}\right), \left(\frac{Vs_x}{Vs_{1,1}}\right)\}, \quad \text{with} \quad P_x \subset Pnor_x, \quad \text{and} \quad P_x \leq 3 + 6\sum_{m=1}^{n=x-1} \frac{Vs_m}{Vs_{1,1}}, x \geq 2; \tag{11}$$

Distinct weighting ratios P_x defined according to expression equation reference goes here Eq. (11) can be found in Table 1 from the sum ($\xi_{x,j=1}$+$\xi_{x,j=2}$). Parameter $\xi_{x,j}$ defines how $Vs_{x,j}$ increases in the proposed topology with x cells.

According to the modes represented in Table 1, it is possible to obtain n different levels for the inverter output voltage from $\xi_{x,j}$.

Other configurations proposed in this work that allow the better distribution of voltage stresses across the switches are defined as follows ($Vs_{1,1}$,$Vs_{1,2}$; $Vs_{2,1}$,$Vs_{2,2}$): (1) 31 levels—$Vs_{1,1}$, $5Vs_{1,1}$; $3Vs_{1,1}$, $9Vs_{1,1}$; (2) 35 levels—$Vs_{1,1}$, $9Vs_{1,1}$; $5Vs_{1,1}$, $7Vs_{1,1}$; (3) 39 levels—$Vs_{1,1}$, $5Vs_{1,1}$; $8Vs_{1,1}$, $10Vs_{1,1}$; (4) 33 levels—$Vs_{1,1}$, $10Vs_{1,1}$; $8Vs_{1,1}$, $5Vs_{1,1}$; (5) 33 levels—$Vs_{1,1}$, $8Vs_{1,1}$; $4Vs_{1,1}$, $11Vs_{1,1}$. As it was mentioned before, they are able to produce a maximum number of equally-spaced levels for the output voltage by using only two cells, thus making the converter prominent for high-voltage applications.

Table 2 shows a comparison among the operation modes presented in Table 1 and the conventional topologies.

Among the modes presented in Tables 1 and 2, a configuration defined as (1:2:7:14) was chosen for the implementation of the topology shown in Fig. 2, since it uses reduced component number to provide the desired number of levels.

Fig. 3 presents the generic form of the circuit depicted in Fig. 2 for the inverter operating with x CHB-2bs cells.

This representation shows that the inverter is able to operate with two possible configurations for $Vs_{x,j}$. Case 1 includes the possibility of using independent dc voltage sources, where the x-th CHB-2bs cell is supplied by a dc voltage $Vs_{x,j}$ whose magnitude is $\xi_{x,j}.Vs_{1,1}$. In case 2, it is possible to use $Vs_{x,j}$ as an ac voltage source, which can be obtained by using a transformer arranged according to Fig. 2. The maximum value of $Vs_{x,j}$ in this arrangement depends on parameter $\xi_{x,j}$, the number of levels n, and the peak value of the desired sinusoidal output voltage V_{po}. The inverter operation

Table 1
Proposed topology—configurations versus parameter $\xi_{x,j}$.

Mode	Configuration	$\xi_{x,j}$
I	1:2:4:8:16:32…	$2^{2(x-1)+(j-1)}$
II	1:2:7:14:28:56…	$2^{2(x-1)+(j-1)} \cdot 7, x \geq 2$
III	1:2:7:14:49:98…	$2^{(j-1)} \cdot 7^{(x-1)}$

Table 2
Asymmetrical topologies versus number of levels.

Comparison among asymmetrical topologies						
Cells		Config.	1	2	3	x
Number of levels	CHB	Binary	3	7	15	$2^{x+1}-1$
		Ternary	3	9	27	3^x
	CHB-2bs	Mode I	7	31	63	$2^{2x}-1$
		Mode II	7	49	217	$7 \cdot (2^{2x-1}-1)$
		Mode III	7	49	343	7^x

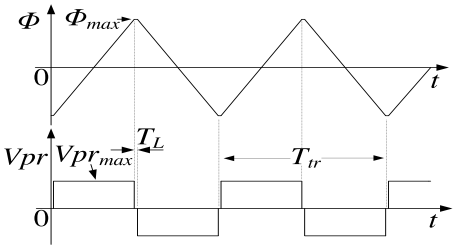

Fig. 4. Waveform representing the voltage across the primary winding Vpr and its respective magnetic flux Φ.

in case 2 is analyzed in this work, whose advantages have been previously mentioned.

According to the topology proposed in Figs. 2 and 3 and considering that double gating signals are applied to switch $Sxyz$ following the restrictions imposed by Eq. (9), while omitting the term z in the nomenclature due to the simultaneous drive, $Sx2$ can be defined as a NOR function of $Sx1$ and $Sx5$, as switch $Sx4$ becomes a NOR function of $Sx3$ and $Sx6$. Besides, $Sxy = 1$ and $Sxy = 0$ correspond to states when the switch is on and off, respectively.

Thus, the output voltage expressed in terms of a switching function for the multilevel inverter operating in case 1 as shown in Fig. 3(a) is given by:

$$Vo = Vs_{1,1} \cdot \sum_{x=1}^{x} \left[(\xi_{x,j=1} + \xi_{x,j=2})(Sx1 - Sx3) + \xi_{x,j=2}(Sx5 - Sx6)\right] \tag{12}$$

According to Eq. (12), the output voltage can be controlled depending only on four switches per CHB-2bs cell. The switching frequencies for the chosen configuration (1:2:7:14) of the inverter represented in Fig. 3 operating in case 1 and employing dc voltage sources with staircase modulation are defined by:

$$\begin{aligned} F_{sx1 \text{ and } sx3} &= (2^{2(xt-xd)+3} - 5)f_1 \\ F_{sx5 \text{ and } sx6} &= (2^{2(xt-xd)+3} - 4)f_1 \\ F_{sx2 \text{ and } sx4} &= (2^{2(xt-xd)+2} - 3)f_1 \end{aligned} \tag{13}$$

where xt is the total amount of series-connected CHB-2bs cells and xd corresponds to the position of the desired cell.

The expressions in Eq. (13) are the referential basis for the comparison of switching frequencies in the inverter implemented with ac voltage sources i.e., case 2 in Fig. 3, which will be discussed in the next section.

Session 5 is concerned with evaluating how the increase of the transformer operating frequency is supposed to affect the switching frequencies in the inverter presented in Fig. 2.

5. Operation of the multilevel inverter with ac–ac stage

5.1. Transformer

Based on Fig. 2, it is possible to notice that the voltage across the primary winding with Npr turns can be expressed as a switching function given by $Vpri = V_{in}(Si1–Si3)$. This voltage appears across the secondary windings with $Ns_{x,j}$ turns as defined by $Vs_{x,j} = (Ns_{x,j}/Npr).[V_{in}(Si1–Si3)]$.

The waveform in Fig. 4 represents the practical implementation of the proposed multilevel inverter, while voltage Vpr can be measured across the primary winding.

According to Fig. 4, the relationship between the magnetic flux measured in maxwell with the waveform of the voltage across the primary winding *Vpr* is defined in Eqs. (14) and (15).

$$Vpr(t) = N_{pr}\frac{d\phi}{dt}\cdot 10^{-8}(V)$$

$$\begin{cases} Vpr_{\max} = N_{pr}\dfrac{\phi_{\max}}{(1/4)T_{tr}}\cdot 10^{-8}(V), \quad if \quad \dfrac{T_L}{2} \le t \le \dfrac{T_{tr}-T_L}{2}. \\ -Vpr_{\max} = N_{tr}\dfrac{\phi_{\max}}{(1/4)T_{tr}}\cdot 10^{-8}(V), \quad if \quad \dfrac{T_{tr}+T_L}{2} \le t \le \dfrac{2T_{tr}-T_L}{2}. \end{cases} \tag{14}$$

$$\begin{aligned} Vpr_{rms} &= \sqrt{\int_{\frac{T_L}{2}}^{\frac{T_{tr}-T_L}{2}} Vpr_{\max}{}^2 dt + \int_{\frac{T_L+T_{tr}}{2}}^{\frac{2T_{tr}-T_L}{2}} (-Vpr_{\max})^2 dt} \\ &= Vpr_{\max}\sqrt{1-\frac{2T_L}{T_{tr}}} = N_{pr}\frac{\phi_{\max}}{(1/4)T}\sqrt{1-\frac{2T_L}{T_{tr}}}\cdot 10^{-8} \\ &= 4\cdot N_{pr}\cdot f_{tr}\cdot B_{\max}\cdot A_{ef}\cdot\sqrt{1-\frac{2T_L}{T_{tr}}}\cdot 10^{-8} \end{aligned} \tag{15}$$

From expression (15), it is possible to obtain the number of turns of the primary winding as in Eq. (16), where A_{ef} is the core effective cross section area measured in cm^2 and f_{tr} is the transformer operating frequency. Besides, converting gauss to tesla in B_{max} gives:

$$Npr = \frac{Vpr_{rms}\cdot 10^4}{4\cdot N_{pr}\cdot f_{tr}\cdot B_{\max}\cdot A_{ef}\cdot\sqrt{1-\frac{2T_L}{T_{tr}}}} \tag{16}$$

If the number of primary turns *Npr*, the peak-to-peak value of the desired sinusoidal waveform defined as V_{po}, and the input voltage *Vin* are known, the number of secondary turns can be obtained as:

$$Ns_{x,j} = \frac{2^j\cdot 7^{x-1}\cdot V_{po}\cdot Npr}{(n-1)Vin} \tag{17}$$

In order to implement the proposed topology, a grain-oriented silicon–steel toroidal core has been employed in the transformer considering the following parameters: flux density $B_{max} = 0.68$ T, operating frequency $f_{tr} = 300$ Hz, and $A_{ef} = 7.75\ cm^2$, with dimensions 102 mm × 134 mm × 51 mm (inside diameter—ID × outside diameter—OD × height—H), sheets of 0.27 mm, and stacking factor of 0.95.

5.2. Operation of the proposed asymmetrical inverter

The converter output voltage *Vo* corresponds to the combination of voltages across the secondary windings $Vs_{x,j}$ defined by a switching function expressed as:

$$Vo = \underbrace{(Si - Si3)}_{p}\frac{2.V_{po}}{n-1}\cdot \sum_{x=1}^{x}\cdot \underbrace{\left[(\xi_{x,j=1}+\xi_{x,j=2})\cdot(Sx1-Sx3)+\xi_{x,j=2}\cdot(Sx5-Sx6)\right]}_{q} \tag{18}$$

According to Eq. (18), a particular switching configuration is necessary to obtain either positive or negative values of the output voltage for each one of the states for voltage *Vpr* (positive or negative), thus resulting in a desired level *n*. In general, the following equality must be maintained: *Sign*(*p*).*Sign*(*q*) = *Sign*(*Vo*). If *Sign*(*p*) = 0, *q* remains the same.

Therefore, if a hypothetical example of the proposed inverter operating with 25-level output voltage is chosen, the switching states defined in Fig. 5 are valid.

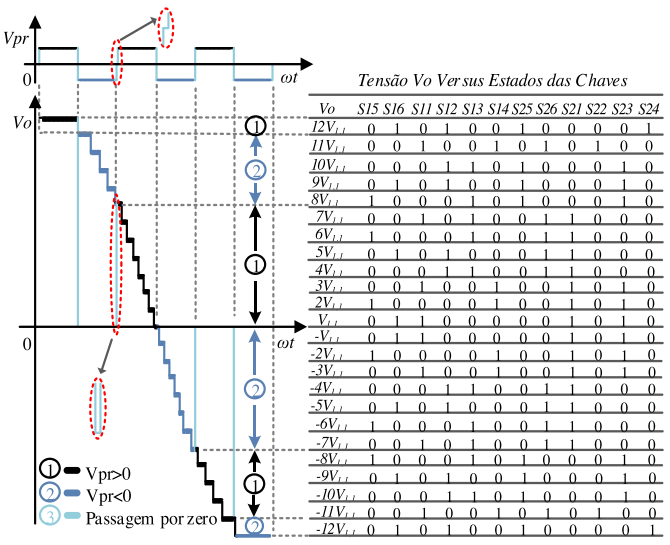

Fig. 5. Composition of the output voltage waveform based on the primary voltage *Vpr* for the inverter employing an ac–ac stage and configuration (1:2:7:14).

If the voltage across the HB is positive i.e., *Vpr* > 0 and the desired voltage is also positive i.e., *Vo* > 0 to generate level +*n* as in Eq. (18), then *p* > 0 and *q* > 0. If the voltage across HB becomes negative for *Vo* > 0, then *p* < 0 and *q* < 0 so that the symmetrical state +*n* is obtained, thus keeping *Vo* unchanged. This case is shown in Fig. 5 when the switching states change from $12\,V_{1,1}$ to $11\,V_{1,1}$.

Fig. 5 presents the output voltage waveform and its composition as influenced by the primary voltage and the inverter switching states. Discontinuities can be seen in voltage *Vo*, which result from the zero-crossing interval of the HB. However, they can be promptly eliminated by using an output filter.

Fig. 5 also shows the switching states (*Sxy* = 1 → *Sxya* is on and *Sxyb* is on) necessary for the generation of levels. The state defined as *Sxy* = 0 corresponds to turning on a given switch depending on the polarity of *Vpr* and turning off another switch that is part of the corresponding pair *Sxya* or *Sxyb*.

This work has considered the optimum case for the level transition, where one state avoids eventual short-circuit through voltage sources $Vs_{x,1}$ and $Vs_{x,2}$.

Table 3 presents the transition states regarding one eighth of the output voltage cycle, which comprehends seven distinct states for the fundamental component Vo_{h1}. Besides, *R* and *S* represent the (*R*/*S*) states valid for *Vpr* > 0 and *Vpr* < 0, respectively.

In order to check the switching frequency of the independent switches (*Sxya* or *Sxyb*) that are part of the bidirectional switch, Table 4 was obtained for different values for the operating frequency of the transformer represented by f_{tr}.

It can be seen that the switches in the cell that processes the lowest amount of power (*S1yz*) operate with higher frequency, while the cell that processes the highest amount of power (*S2yz*) present lower switching frequency, which contributes drastically to the reduction of switching losses.

The first row containing the ratio between the switching frequency and the fundamental frequency ($F_{sxy}/f1$) represents an important benchmark since it refers to the implementation of the inverter using dc voltage sources (No f_{tr}).

This prominent behavior shows that the switches in the first cell are not significantly affected by the operating frequency of the transformer even when it is assumed to be 1800 Hz, considering that the switching frequencies for *S1yz* are very close to the case where the inverter operates with dc voltage sources. On the other hand, the switches in the cell processing the highest power (*S2yz*)

Table 3
Transition states for the first CHB-2bs cell.

Switches vs voltage *Vo*												
S15a	S15b	S16a	S16b	S11a	S11b	S12a	S12b	S13a	S13b	S14a	S14b	*Vo*
1/0	0/1	1/0	0/1	1/1	1/1	0/1	1/0	1/1	1/1	0/1	1/0	0
1/0	0/1	1/0	0/1	1/1	1/0	0/1	1/0	0/1	1/1	0/1	1/0	$V_{1,1}$
1/1	0/0	0/0	1/1	0/1	1/0	0/1	1/0	0/1	1/0	0/1	1/0	$2V_{1,1}$
1/1	0/0	0/0	1/1	0/1	1/0	0/1	1/1	0/1	1/0	1/1	1/0	$3V_{1,1}$
0/0	0/0	0/0	0/0	0/1	1/0	0/1	1/0	0/1	1/0	0/1	1/0	$4V_{1,1}$
0/0	1/1	1/1	0/0	0/1	1/0	1/1	1/0	0/1	1/0	0/1	1/1	$5V_{1,1}$
0/0	1/1	1/1	0/0	0/1	1/0	0/1	1/0	0/1	1/0	0/1	1/0	$6V_{1,1}$

Table 4
Switching frequency for independent switch *Sxya* or *Sxyb*.

Operation modes		Frequency ratio *Fsxy/f1*					
f_{tr}	$f_{tr}/f1$	S15 *a/b*	S16 *a/b*	S11 *a/b*	S13 *a/b*	S12 *a/b*	S14 *a/b*
No f_{tr} (1)	xxx	28	28	27	27	13	13
f_{tr} = 300 Hz	5	23	24	15	14	11	10
f_{tr} = 600 Hz	10	27	27	18	18	14	14
f_{tr} = 1200 Hz	20	28	28	22	21	20	20
f_{tr} = 1800 Hz	30	33	33	30	30	25	25

No f_{tr} (1): this condition refers to the inverter operating with dc voltage *Vdc* supplying the CHB-2bs cells (i.e., f_{tr} = 0). *f*1 was adopted 60 Hz.

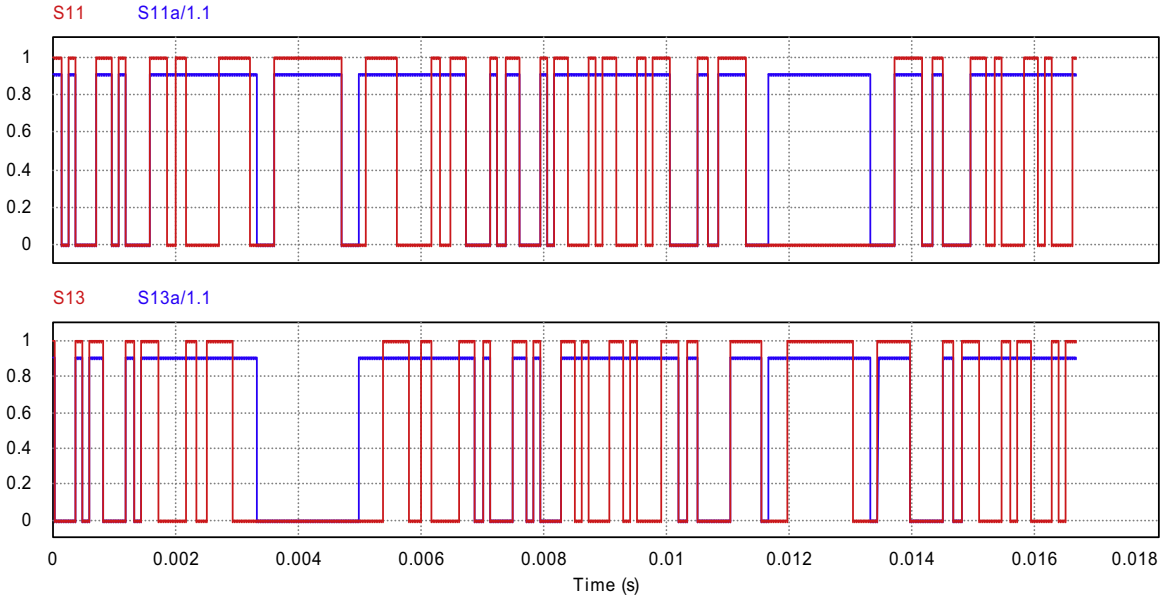

Fig. 6. Comparison among switching frequencies: (a) S11 and S13 correspond to the inverter operation with dc voltage sources and (b) S11a and S13a correspond to the inverter operation with ac voltage sources at 300 Hz.

operate with switching frequencies lower than that of the transformer. Besides, a significant reduction of the frequency ratio with respect the operation at 1800 Hz can be verified.

An example obtained by simulation shows the gating pulses for switches *S*11 and S13 while the inverter operates with dc voltage sources, and also the gating pulses applied to *S*11a and *S*13a where the inverter employs a transformer operating at 300 Hz considering one cycle of the output voltage in Fig. 6. It can be seen that switches *S*11*a* and *S*13*a* operate with lower frequency in this case.

Table 5 shows the THD of the output voltage *Vo* (before the filter) for different values of the transformer frequency operating with T_L = 2us.

5.3. Power processed by the asymmetrical inverter

The maximum value of the fundamental output voltage $Vo_{f1}^{\max}$, Fig. 7 that can be assumed by the inverter can be expressed in terms of a Fourier series as shown in Eqs. (1)–(3). Finally, it is possible to rewrite it in Eq. (4) knowing that term V_{dc} can be expressed as a function of the maximum voltage that can be assumed by the second cell, resulting in Eq. (19).

$$Vo_{f1}^{\max} = \frac{4V_{dc}}{\pi}\cdot\left[\cos\left(\sin^{-1}\frac{1}{7^x}\right)+\cos\left(\sin^{-1}\frac{3}{7^x}\right)+\cdots\cos\left(\sin^{-1}\frac{7^x-2}{7^x}\right)\right] = \frac{4}{\pi}\frac{Vo_{h2}^{\max}}{3\cdot 7^{x-1}}\cos\left[\sin^{-1}\left(\frac{2i+1}{7^x}\right)\right]\sum_{i=0}^{\frac{7^x-1}{2}-1} \tag{19}$$

Fig. 7 shows the waveforms of the voltages across the output sides of the CHB-2bs cells, as well as the respective maximum values of their fundamental components, the output voltage *Vo*(*t*) and its corresponding fundamental component Vo_{f1}, and also its respective maximum value i.e., $(Vo)_{f1}^{\max}$ = 100%.

Table 5
Transformer frequency versus THD (Vo) for $T_L = 2\,\mu s$.

f_{tr}	300 Hz	600 Hz	1200 Hz	1800 Hz
THD (Vo)	4.03%	5.32%	7.24%	8.77%

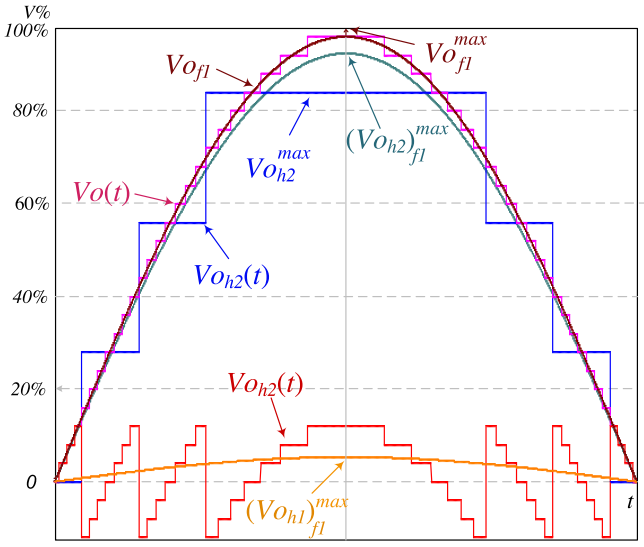

Fig. 7. Relevant waveforms (a) output voltage $Vo(t)$, (b) voltage across the second cell $Vo_{h2}(t)$ and (c) voltage across the first cell $Vo_{h1}(t)$ and respective maximum values of the fundamental components $(Vo_{h2})_{f1}^{max}$ and $(Vo_{h1})_{f1}^{max}$.

In order to obtain the maximum fundamental components of the output voltage across the cells, expression (20) can be employed.

$$(Vo_{hxd})_{f1}^{max} = \begin{cases} Vo_{f1}^{max}|^{x=xt-xd+1}, & \text{for } x_d = x_t, \\ Vo_{f1}^{max}|^{x=xt-xd+1} - Vo_{f1}^{max}|^{x=xt-xd}, & \text{for } x_d \neq x_t \end{cases} \quad (20)$$

The second statement shown in Eq. (20) can be seen graphically in Fig. 7 for the inverter operating with two cells ($xt = 2$), when it is desired to obtain the maximum fundamental component of the first cell ($xd = 1$), which is expressed as $Vo_{f1}^{max}|^{x=2} - Vo_{f1}^{max}|^{x=1}$.

The power processed by the inverter Po can be written according to Eq. (21), where $(Vo_{hxd})_{f1}^{rms}$ and $(Io_{hxd})_{f1}^{rms}$ correspond to the rms values of the fundamental components of the output voltage and output current in cell xd, respectively, and ϕ is the phase shift angle.

$$Po = \frac{1}{T}\int_o^T i_o(t)v_o(t)dt = \sum_{xd=1}^{x}(Vo_{hxd})_{f1}^{rms} \cdot (Io_{hxd})_{f1}^{rms}.\cos\phi \quad (21)$$

Since the CHB-2bs cells are connected in series, the current flowing through them is equal to the load current i.e., $(Io_{h1})_{f1}^{rms} = (Io_{h2})_{f1}^{rms} = (Io)_{f1}^{rms}$. It is also known that the voltages across the cell outputs Vo_{h1} and Vo_{h2} in Fig. 7 are in phase and therefore the same power factor exists in this case. Thus, taking into account the aforementioned statements, it can be concluded according to Eq. (21) that the output power Po is the sum of powers processed by the CHB-2bs cells as the inverter power distribution is associated with term $(Vo_{hxd})_{f1}^{rms}$ only, which is the rms value of the fundamental component of the output voltage for each CHB-2bs cell (xdth).

Table 6 summarizes the operating features of the proposed multilevel inverter.

Table 5 shows that most power is processed by the second cell, which corresponds to 95% of the output power, while the first cell is responsible for processing only 5%. It is worth to mention that the cell that processes the highest amount of power operates at low frequency and vice versa. This characteristic is quite prominent for high-power applications considering that switching losses are reduced and the converter efficiency is significantly increased.

Table 6
Power processing profile of the proposed inverter.

Description	Voltages (V)	Processed power (%)
Second *CHB-2bs* cell	$(Vo_{h2})_{f1}^{max} = 1.10 \cdot Vo_{h2}^{max}$	95%[a]
First *CHB-2bs* cell	$(Vo_{h1})_{f1}^{max} = 0.06 \cdot Vo_{h2}^{max}$	5%[a]
Inverter output	$Vo_{f1}^{max} = 1.16 \cdot Vo_{h2}^{max}$	100%

[a] Ratio given by $\frac{P_{hxd}}{Po} = \frac{(Vo_{hxd})_{f1}^{max}}{Vo_{f1}^{max}}$, where P_{hxd} is the power processed by the desired cell xd, as $xd = 1$ and $xd = 2$ for the first and second cells, respectively.

6. Comparison with other inverter topologies

Considering the aforementioned aspects, it can be stated that CHB-symmetrical inverter in Ref. [33] presents reduced component count compared with conventional topologies such as neutral point clamped (NPC) and flying capacitor (FC). It is also known that the number of active switches (on switches) per synthesized levels in the conventional NPC, FC, and CHB-symmetrical topologies is the same. Thus, this work has adopted the CHB-symmetrical inverter as a reference to compare it in terms of the number of on switches in the proposed topology.

Fig. 8 shows a comparison between the classical CHB-symmetrical inverter topology using independent voltage sources and the proposed one considering the number of on switches.

As it can be seen in Fig. 8, the common point to the three curves shows the same number of on components (i.e., six switches) considering that all inverters operate with seven levels. Besides the CHB-symmetrical inverter in this case operates with three independent voltage sources, while the proposed solution uses a single dc voltage for the whole operating range defined in the graph.

Fig. 8 also shows that the number of on components increases significantly as the number of levels becomes higher than seven in the CHB-symmetrical inverter if compared with the remaining approaches.

Fig. 9 presents a comparison among the proposed solution, the CHB-Binary ac–ac inverter, and the CHB-Ternary ac–ac inverter employing a HB with multi-winding transformer in order to obtain the voltage sources for the cells. It can be seen that 10 switches must be turned on to generate seven levels in both the CHB-Binary ac–ac and CHB-Ternary ac–ac inverters. However, the proposed one requires only six on switches in this case. Besides, it can be stated the number of on components is drastically reduced as the number of levels increases when comparing with the other configurations.

7. Experimental results

The laboratory prototype shown in Fig. 10 was implemented to validate the whole theoretical analysis. The converter design includes a multi-winding transformer operating at 300 Hz, while the input voltage $Vin = 48$ V.

The inverter supervisory system was developed in an FPGA (field programmable gate array) model Ciclone IV EP4CE22F17C6N manufactured by Altera.

Since the external crystal that powers the FPGA operates at 50 MHz, an internal phase-locked loop (PLL) module was employed to obtain a clock frequency which is a multiple of the inverter operating frequency so that internal mathematical operations could be performed without error accumulation.

The reference clock signal provided by the PLL module is 60 MHz. The clock signals for other peripherals as well as that for the analog-to-digital converter (ADC) was obtained using 60-MHz clock frequency dividers. In addition, in order to ensure the accurate

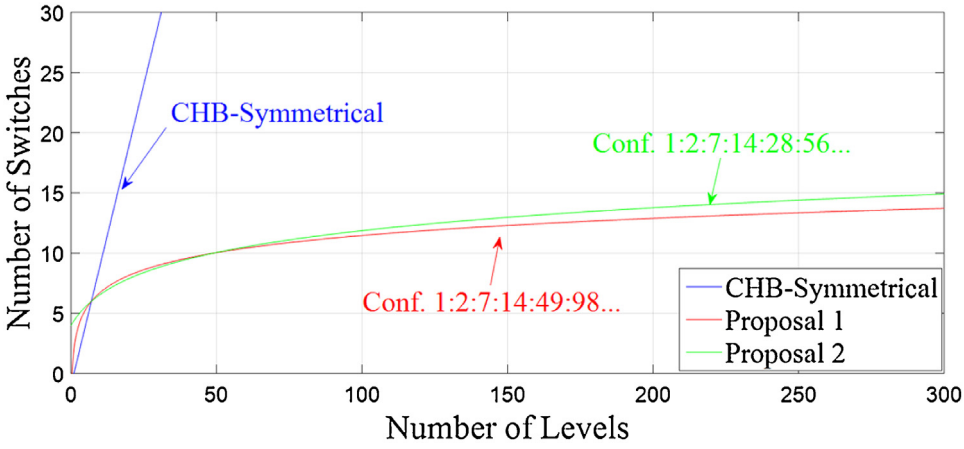

Fig. 8. Comparison between the CHB inverter and the proposed topology considering the number of on switches per number of synthesized levels.

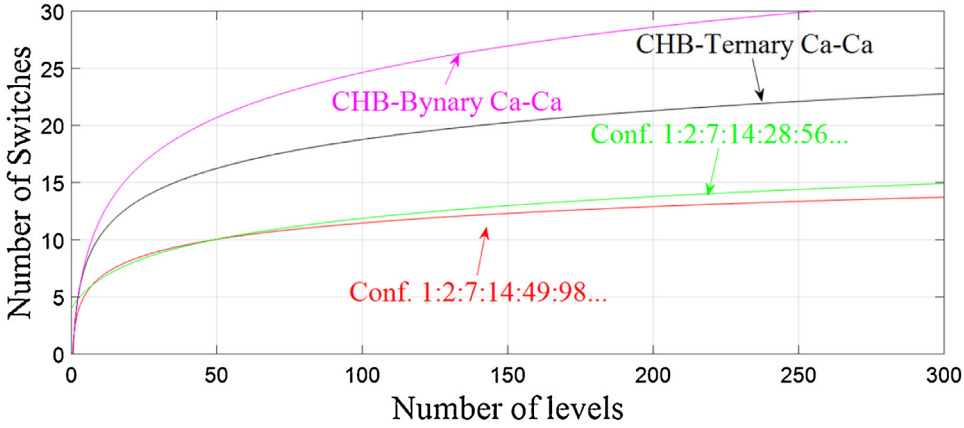

Fig. 9. Comparison among the proposed approach, the CHB-Bynary ac–ac inverter, and the CHB-Ternary ac–ac inverter considering the number of on switches per number of synthesized levels.

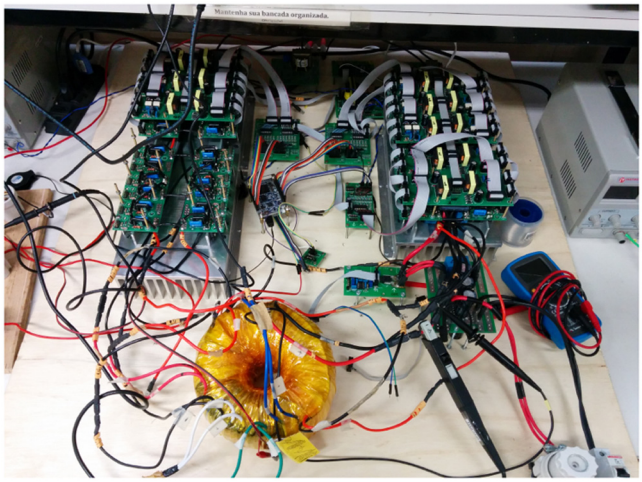

Fig. 10. Experimental: prototype of the bidirectional multilevel converter with ac–ac stage.

prototype operation, the code developed in VHDL (virtual hardware description language) must define the operating frequency of the transformer f_{tr} as a multiple of the output frequency *f1*. It is worth to mention that the commutation of the switches in the *CHB-2bs* cells must occur when $Vpr = 0$ V in order to ensure the desired voltage *Vo* when the polarity of the voltage across the primary winding is reversed so that short-circuit is avoided.

The prototype was evaluated considering an input voltage $V_{in} = 48$ V, rms output voltage $Vo = 220$ V and output power $Po = 600$ W when the inverter supplies an RL (resistor–inductor) load ($R_o = 77.4\,\Omega$, $L_o = 19.2$ mH).

The contribution of each CHB-2bs cell for the achievement of 49 levels in the desired waveform is shown in Fig. 11.

Fig. 12 is shown the current in the primary winding controlled and without spikes, which validates the implementation.

According to Figs. 11 and 12, the resulting waveform does not present voltage spikes during the level transition, thus validating the successful application of optimum switching states for the inverter operation with inductive loads.

The existing discontinuities in the voltage waveforms represented in Figs. 11–13 are due to the zero-crossing interval corresponding to $T_L = 2\,\mu$s, which is used by the HB that supplies the transformer primary winding. However they can be attenuated by reducing T_L and using a proper output filter.

8. Conclusions

This paper has presented a new bidirectional multilevel inverter using a multi-winding power transformer. The transformer stage operates at medium frequency, thus reducing the overall converter size and volume when compared to other topologies operating at low frequency. Optimum switching states could be derived for the proposed inverter, thus allowing the operation with inductive loads without short-circuit issues.

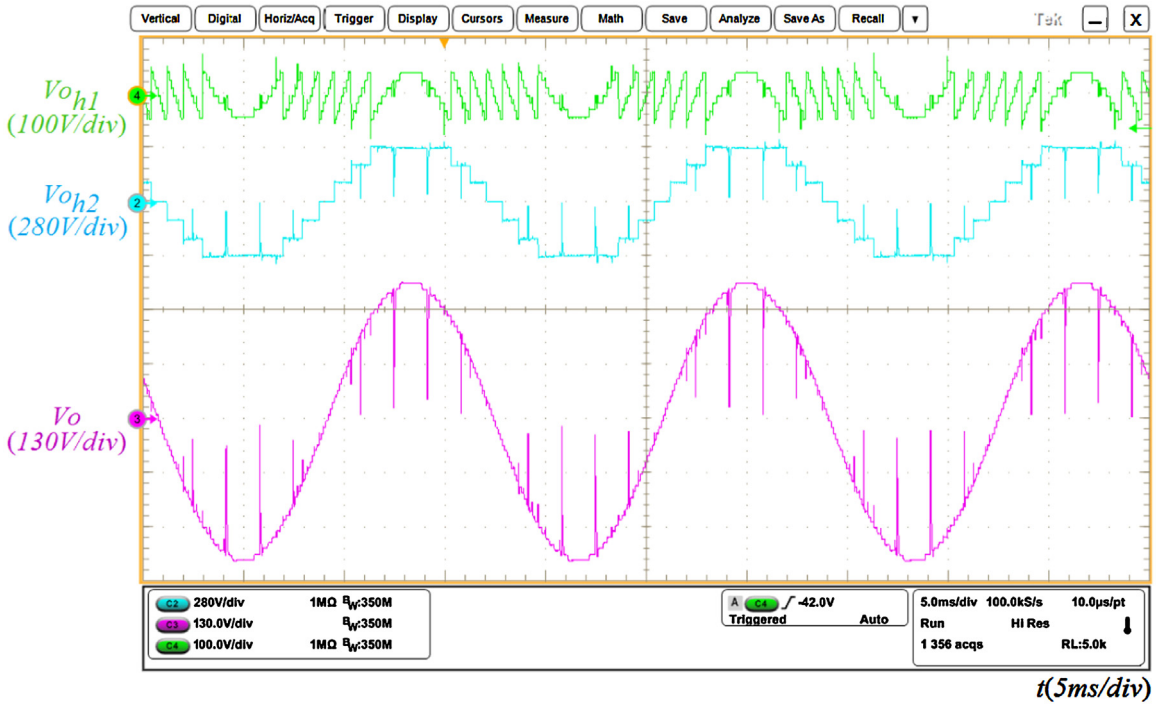

Fig. 11. Waveforms in the inverter output stage. Voltages Vo_{h1} and Vo_{h2} across the first and second CHB-2bs cells, respectively, and 49-level output voltage without filtering.

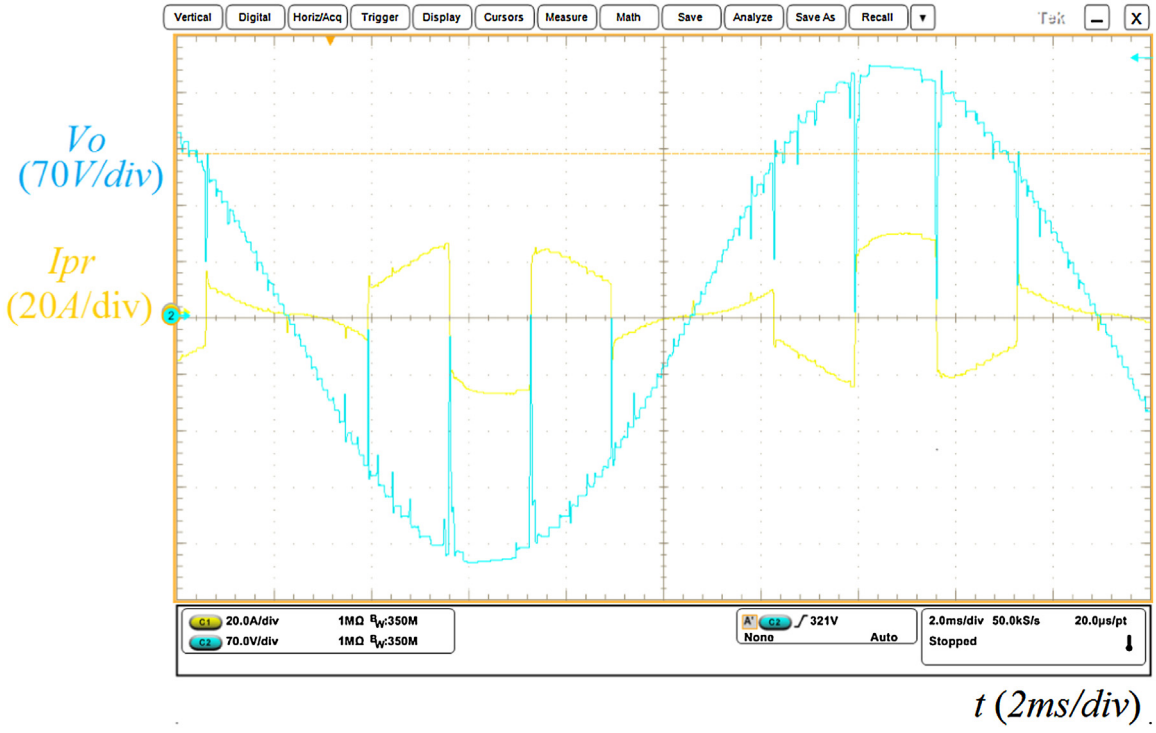

Fig. 12. Output voltage *Vo* and current *Ipr* controlled in the primary winding.

The comparison involving the proposed approach and other conventional multilevel topologies has shown the significant reduction in the number of on state semiconductors.

The theoretical analysis carried out in this work has determined how the power processed by the inverter is effectively distributed, as it was shown that the first and second cells are responsible for processing 5% and 95% of the output power, respectively. Within this context, the analysis of the switching frequency for the operation with an ac–ac stage has shown that cells that process the higher amounts of power operate at lower frequencies, thus contributing to the minimization of switching losses.

Besides, an interesting behavior could be verified when investigating different values for the transformer operating frequency, even when it operates at 1800 Hz. In this case, the switching frequency for the switches in the first CHB-2bs cell is nearly the same as that when the inverter operates with dc voltage sources. Con-

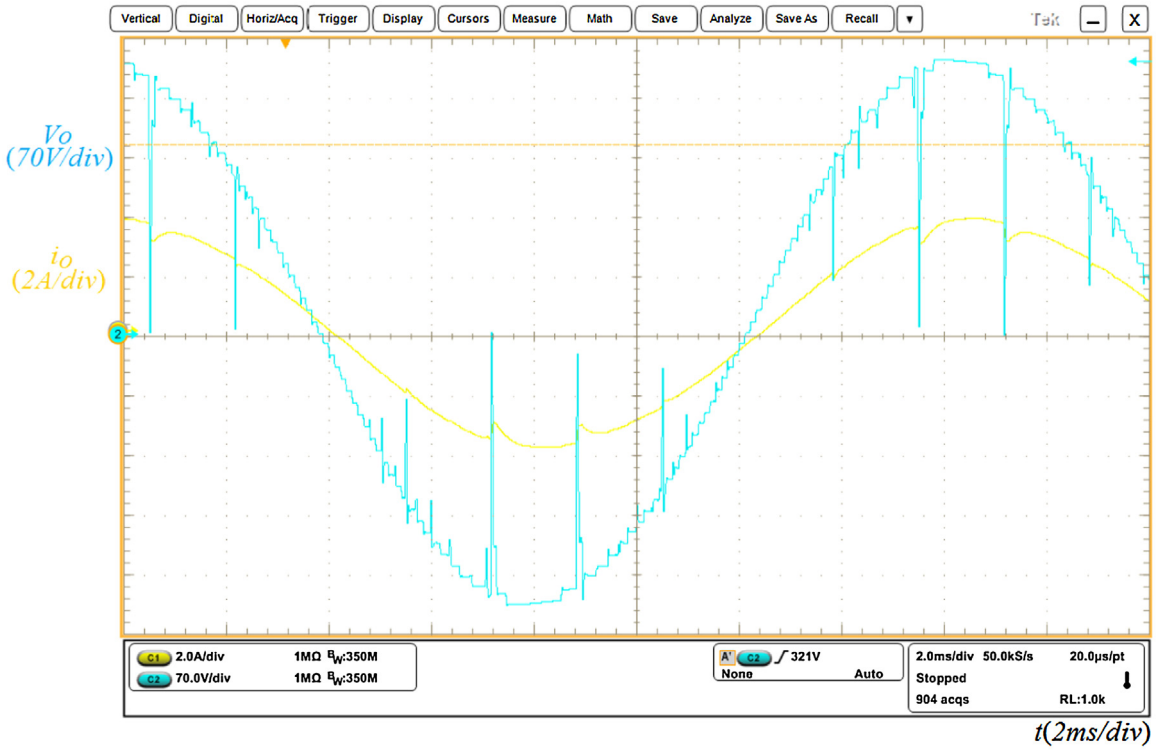

Fig. 13. Output voltage and load current for the inverter supplying a *RL* load.

sidering the analyzed range, the switches in the cell that processes the highest amount of power have always presented switching frequencies lower than the transformer operating frequency. The central switches of the aforementioned cell corresponding to *S25z* and *S26z* operate at a frequency that is 33% of the transformer operating frequency even at 1800 Hz. This characteristic operation shows that it is possible to reduce the inverter volume without significant impact on switching losses.

It can be stated that the introduced inverter is promising for applications to standalone PV systems and appropriate interfacing in dc–ac microgrids due to minimized losses and increased robustness. The use of topologies with high resolution of the output voltage employing few components is promising since there is the possibility of eliminating the dc–dc converter to supply the inverter and regulating the load voltage by controlling the number of levels only. The proposed structure is also able to operate with high power density, which reduces the cost of implementing bulky filters and also introduces an approach that is also for adequate low-power applications.

Acknowledgments

The authors acknowledge CAPES for the financial support and UFC for providing overall support to this work.

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