Novel Nonisolated High-Voltage Gain DC–DC Converters Based on 3SSC and VMC

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***Abstract*—This paper introduces a new family of dc–dc converters based on the three-state switching cell and voltage multiplier cells. A brief literature review is presented to demonstrate some advantages and inherent limitations of several topologies that are typically used in voltage step-up applications. In order to verify the operation principle of this family, the boost converter is chosen and investigated in detail. The behavior of the converter is analyzed through an extensive theoretical analysis, while its performance is investigated by experimental results obtained from a 1-kW laboratory prototype and relevant issues are discussed. The analyzed converter can be applied in uninterruptible power supplies, fuel cell systems, and is also adequate to operate as a high-gain boost stage with cascaded inverters in renewable energy systems. Furthermore, it is suitable in cases where dc voltage step-up is demanded, such as electrical fork-lift, audio amplifiers, and many other applications.**

***Index Terms*—Boost converters, dc–dc converters, high voltage gain, voltage multiplier cells (VMCs).**

I. Introduction

DEPENDING on the application nature, several types of static power converters are necessary for the adequate conversion and conditioning of the energy provided by primary sources such as photovoltaic arrays, wind turbines, and fuel cells. Besides, considering that the overall cost of renewable energy systems is high, the use of high-efficiency power electronic converters is a must [1].

The literature presents numerous examples for applications where dc–dc step-up stages are necessary, e.g., audio amplifiers [2], uninterruptible power supplies (UPSs) [3], fuel cell powered systems [4], and fork lift vehicles [5], although many other ones can be easily found. Typical solutions include the use of low-frequency or high-frequency power transformers to adjust the voltage gain properly. Besides, galvanic isolation may be necessary due to safety reasons [6]. Unfortunately, this practice may bring increased size, weight, and volume if compared with nonisolated approaches such as the boost converter.

The conventional boost converter can be advantageous for step-up applications that do not demand very high voltage gain, mainly due to the resulting low conduction loss and design simplicity [7]. Theoretically, the boost converter static gain tends to be infinite when duty cycle also tends to unity. However, in practical terms, such gain is limited by the I^2R loss in the boost inductor due to its intrinsic resistance, leading to the necessity of accurate and high-cost drive circuitry for the active switch, mainly because great variations in the duty cycle will affect the output voltage directly [8].

Due to the importance of the conventional boost converter in obtaining distinct and improved topologies for voltage step-up applications, some techniques have been developed and modified with the aim of improving the characteristics of the original structure. Basically, two strategies are adopted for this purpose: voltage step-up with and without using extreme values of duty cycle. Some arrangements available in the literature will be discussed as follows.

Cascading one or more boost converters may be considered to obtain high voltage gain. Even though more than one power processing stage exists, the operation in continuous conduction mode (CCM) may still lead to high efficiency [9]. The main drawbacks in this case are increased complexity and the need for two sets that include active switches, magnetics, and controllers. Besides, the controllers must be synchronized and stability is of great concern [10]. Due to high power levels and high output voltage, the latter cascaded boost stage has severe reverse losses, with consequent low efficiency and high electromagnetic interference (EMI) levels. Typical examples of such topologies are the single-switch quadratic boost converter and the two-switch three-level boost converter [11].

Converters with magnetically coupled inductance such as flyback or the single-ended primary inductance converter (SEPIC) can easily achieve high voltage gain using switches with reduced on-resistance, even though efficiency is compromised by the losses due to the leakage inductance [12]. An active clamping circuit is able to regenerate the leakage energy, at the cost of increased complexity and some loss in the auxiliary circuit [13].

A hybrid boost–flyback converter is introduced in [14]. The efficiency of the conventional flyback structure is typically low due to the parasitic inductance. A possible solution lies in connecting the output of the boost converter to that of the flyback topology, with consequent increase of voltage gain due to the existent coupling between the arrangements. In this case, the boost convert behaves as an active clamping circuit when the main switch of the flyback stage is turned OFF.

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A boost converter using switched capacitors is proposed in [15], where high voltage gain can be obtained, but it is restricted to low-power applications. In this case, the dc output voltage can be increased as desired by adding a given number of capacitors. Low duty cycle is used, alleviating the problem of the boost diode reverse recovery. However, the high component count with distinct ratings is an inherent drawback.

As the power rating increases, it is often required to associate converters in series or in parallel. In high-power applications, interleaving of two boost converters is usually employed to improve performance and reduce size of magnetics. Besides, for high-current applications and voltage step-up, the currents through the switches become just fractions of the input current. Interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, as the size of the energy storage inductors and differential-mode EMI filter in interleaved implementations can be reduced [16]. The converter studied in [17] uses two boost topologies coupled through an autotransformer with unity turns ratio and opposite polarity so that the current is equally shared between the switches. Besides, voltage doubler characteristic is achieved. Even though the current stress through the switches is reduced, the respective voltage stress is less than or equal to half the total output voltage. Isolated drive circuitry must also be employed in this case.

Other topologies using the interleaving technique are investigated in [18]. Voltage multiplier cells (VMCs) are adopted to provide high voltage gain and reduce voltage stress across the semiconductor elements. Interleaving allows the operation of the multiplier stages with reduction of the current stress through the devices. Besides, the size of input inductors and capacitors is drastically reduced. The voltage stress across the main switches is limited to half of the output voltage for a single multiplier stage. However, high component count is necessary, with the addition of a snubber circuit due to the sum of the reverse recovery currents through the multiplier diodes and consequent increase of conduction losses.

The converter described in [19] allows the increase of the static gain by cascading several VMCs that operate based on the resonance principle. It is also shown that the input inductance is the same as that of a conventional boost converter. Even though switching losses are minimized because there is zero-current-switching (ZCS) turn-on of the main switch, conduction losses tend to increase due to the circulating reactive energy.

The topology studied in [20] uses a voltage doubler rectifier as the output stage of an interleaved boost converter with coupled inductors. High voltage gain can be obtained, although efficiency is affected by the use of an resistor-capacitor-diode (RCD) snubber.

In the last few years, some converters based on the three-state switching cell (3SSC) have been proposed, and will be discussed as follows. The 3SSC is obtained by the association of two two-state switching PWM cells (2SSCs) interconnected to a center tap autotransformer, from which a family of dc–dc converters can be derived. This concept was first introduced in [21]. Some prominent advantages can be addressed to such structures, e.g., reduced size, weight, and volume of magnetics, which are designed for twice the switching frequency; the current stress through each main switch is equal to half of the total output current, allowing the use of switches with lower current rating; losses are distributed among the semiconductors, leading to better heat distribution and consequently more efficient use of the heat sinks; the drive circuit of the main switches becomes less complex because they are connected to the same reference node [22].

The topology investigated in [23] uses VMCs associated with the 3SSC, whose claimed advantages are the input current is continuous with low ripple; the input inductor is designed for twice the switching frequency, with consequent weight and volume reduction; the voltage stress across the switches is lower than half of the output voltage, and naturally clamped by one output filter capacitor. As a disadvantage, a small snubber is necessary for each switch and one additional winding per cell is required for the autotransformer [23].

The converter proposed in [24] presents high voltage gain, while the input current is continuous with reduced ripple. The input inductor is also designed for twice the switching frequency, implying reduction of weight and size. The voltage stress through the switches is less than half of the output voltage due to clamping performed by the output filter capacitor. It is also important to mention that, for a given duty cycle, the output voltage can be increased by adjusting the transformer turns ratio without affecting the voltage stress across the main switches. Metal oxide semiconductor field-effect transistors (MOSFETs) with reduced on-resistance can be used to further minimize conduction losses. However, the converter cannot operate adequately when a duty cycle is lower than 0.5 due to magnetic induction issues. The hard commutation of switches and high component count are also possible drawbacks.

An isolated converter, whose characteristics are similar to those of the push–pull converter, is introduced in [25]. The use of the 3SSC is associated with the following advantages: utilization of only one primary winding that allows the addition of a dc current blocking capacitor in series connection, in order to avoid the transformer saturation problem; less copper and reduced magnetic cores are involved during the transformer assembly; and the moderate leakage inductance of the transformer allows the reduction of overvoltage, and the commutation losses of the switches. The autotransformer of the 3SSC has small size, because it is designed for half of the output power and for a high magnetic flux density, since the current through the windings is nearly continuous with low ripple [25].

This paper presents a topology for voltage step-up applications based on the use of multiplier cells constituted by diodes and capacitors. The converter is able to operate in overlapping mode (when a duty cycle D is higher than 0.5) and nonoverlapping mode (when a duty cycle D is lower than 0.5), analogously to other 3SSC-based structures [4], [7], [21]–[25]. However, the study carried out in this paper only considers the operation with $D > 0.5$. The generic structure, which is valid for any number of cells, is initially presented, while the analysis is focused on structures with three cells, aiming to determine the stress regarding the elements that constitute the aforementioned configurations. Experimental results regarding the structure with three multiplier cells are also presented and discussed to validate the proposal.

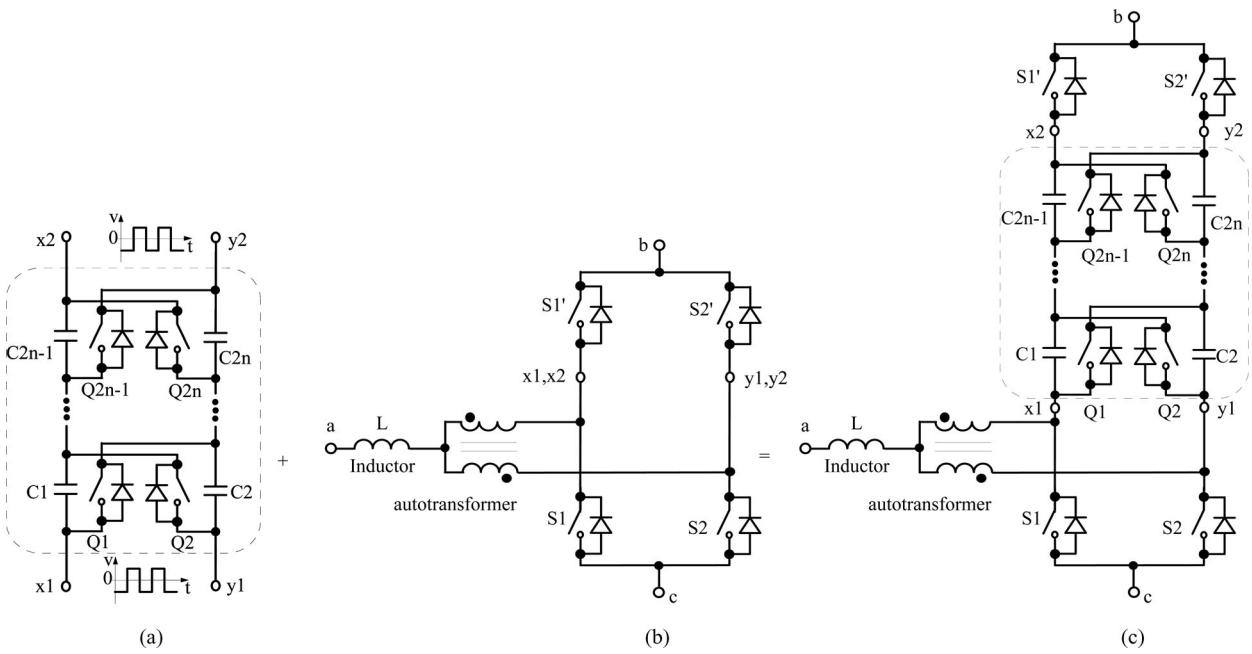

Fig. 1. (a) Voltage multiplier cell. (b) Three-state switching cell. (c) Resulting cell.

II. Proposed Topologies

For good operation of the VMC shown in Fig. 1(a), ac input voltage is required, which is an important requirement of this cell. Due to this fact, the use of the 3SSC depicted in Fig. 1(b) is considered because it generates such ac voltage across the terminals of the autotransformer and the drain terminals of the controlled switches. For this reason, both cells are integrated leading to the proposed cell shown in Fig. 1(c). In the resulting cell, the controlled switches can be represented by MOSFETs, junction field-effect transistors, insulated gate bipolar transistors, bipolar junction transistors, etc. All the generated topologies present bidirectional characteristics.

By using the proposed cell shown in Fig. 1(c), it is possible to generate the six novel nonisolated dc–dc converters, i.e., buck, boost, buck–boost, Cúk, SEPIC, and zeta, which are shown in Fig. 2.

As was mentioned before, the use of high-voltage gain converters is of great interest, even though many approaches are based on isolated topologies [26]–[28]. It is worth to notice that the use of nonisolated converters particularly dedicated to applications regarding renewable power systems has been the scope of recent works [29]–[33]. The efforts leading to the development of such nonisolated topologies are then well justified in the literature.

In order to verify the claimed advantages of the converter family, the boost converter shown in Fig. 2(b) is chosen. The developed analysis considers the converter associated with three voltage multiplier cells and is detailed as follows.

In order to better understand the operating principle of the structures, the following assumptions are made:

1) the input voltage is lower than the output voltage;
2) steady-state operation is considered;
3) semiconductors and magnetics are ideals;
4) switching frequency is constant;
5) the turns ratio of the autotransformer is unity;
6) the drive signals applied to the switches are 180° displaced.

A. Operating Principle

The configuration that uses three multiplier cells is represented in Fig. 3. The equivalent circuits that correspond to the converter operation and the relevant theoretical waveforms are presented in Figs. 4 and 5, respectively.

First stage [t_0, t_1] [see Fig. 4(a)]: Switches S_1 and S_2 are turned ON, while all diodes are reverse biased. Energy is stored in inductor L and there is no energy transfer to the load. The output capacitor provides energy to the load. This stage finishes when switch S_1 is turned OFF.

Second stage [t_1, t_2] [see Fig. 4(b)]: Switch S_1 is turned OFF, while S_2 is still turned ON and diode D_5 is forward biased. There is no energy transfer to the load as well. Inductor L stores energy, capacitors C_1 and C_3 are discharged, and capacitors C_2, C_4, and C_6 are charged.

Third stage [t_2, t_3] [see Fig. 4(c)]: Switches S_1 and S_2 remain turned OFF and ON, respectively. Diodes D_3 and D_7 are forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through D_7. The inductor stores energy, and capacitors C_2 and C_4 are still charged. Capacitors C_1 is discharged, and so are C_3 and C_5.

Fourth stage [t_3, t_4] [see Fig. 4(d)]: Switch S_2 remains turned ON, diode D_3 is reverse biased, and diode D_1 is forward biased. Energy is transferred to the load through D_7. The inductor is discharged, and so are capacitors C_1, C_3, and C_5, while C_2 is charged.

Fifth stage [t_4, t_5] [see Fig. 4(e)]: This stage is identical to the first one.

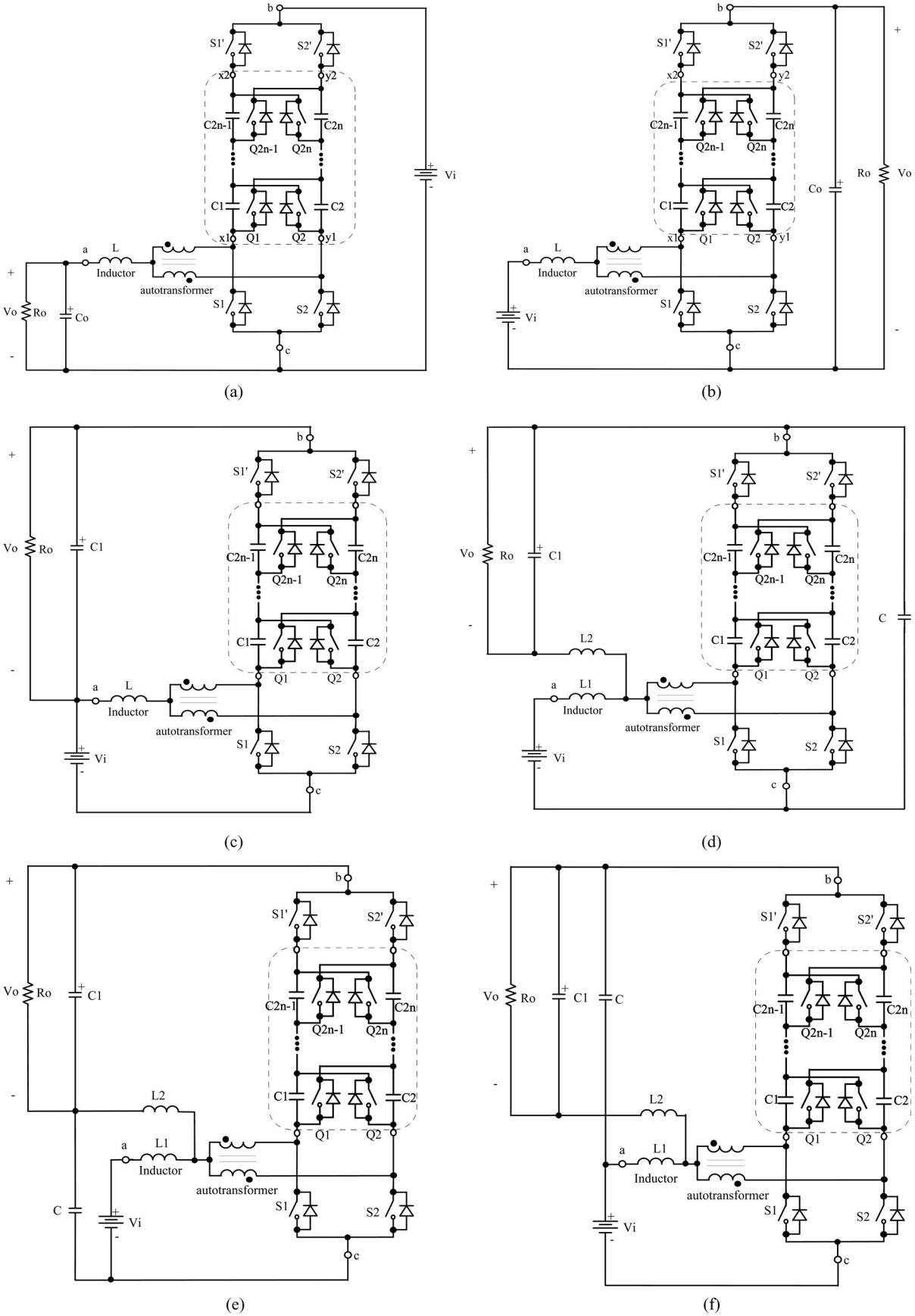

Fig. 2. Nonisolated dc–dc converters using the 3SSC and VMC: (a) buck, (b) boost, (c) buck–boost, (d) Cúk, (e) SEPIC, and (f) zeta.

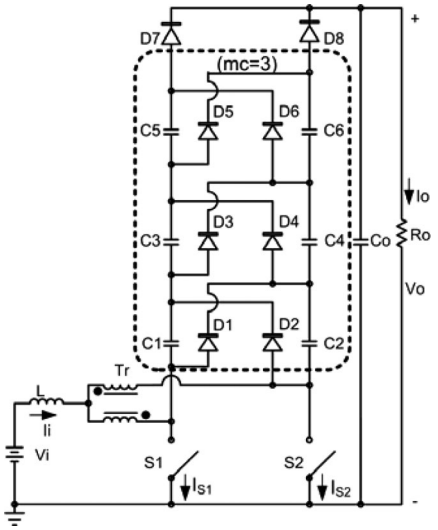

Fig. 3. Proposed boost converter using three VMCs.

Sixth stage [t_5, t_6] [see Fig. 4(f)]: Switch S_2 is turned OFF and switch S_1 is still turned ON. Diode D_6 is forward biased. The inductor is charged by the input source, although capacitors C_2 and C_4 are discharged instead.

Seventh stage [t_6, t_7] [see Fig. 4(g)]: This stage is similar to the third one.

Eighth stage [t_7, t_8] [see Fig. 4(h)]: Switch S_1 is turned ON, while S_2 remains turned OFF. Diodes D_2 and D_8 are forward biased, while D_4 is reverse biased as well as the remaining diodes. Energy transfer to the load occurs through D_8, and capacitor C_o is still charged. The inductor is discharged, while capacitor C_1 is charged and capacitors C_2, C_4, and C_6 are discharged.

B. Static Gain

The static gain for the generic structure of the boost converter can be obtained from the inductor volt–second balance. The voltage area multiplied by the time interval that corresponds to the inductor charge is equal to that regarding the inductor discharged. The following expression can then be derived:

$$G_v = \frac{V_o}{V_i} = \frac{(mc+1)}{(1-D)} \tag{1}$$

where *mc* is the number of voltage multiplier cells; V_i is the input voltage; V_o is the output voltage; and *D* is the duty cycle.

Expression (1) is plotted and shown in Fig. 6, where one can see that the static gain changes when $D<0.5$, as represented by the dotted line. It occurs because the multiplier capacitors are not fully charged due to the reduced charge time.

III. Design Procedure

According to Fig. 6, the static gain of the proposed nonisolated boost converter can be further increased by adding VMCs as necessary, with consequent reduction of voltage stress across the main switches. However, this practice may lead to high component count and also compromise robustness considering that additional diodes and multiplier capacitors are included in the

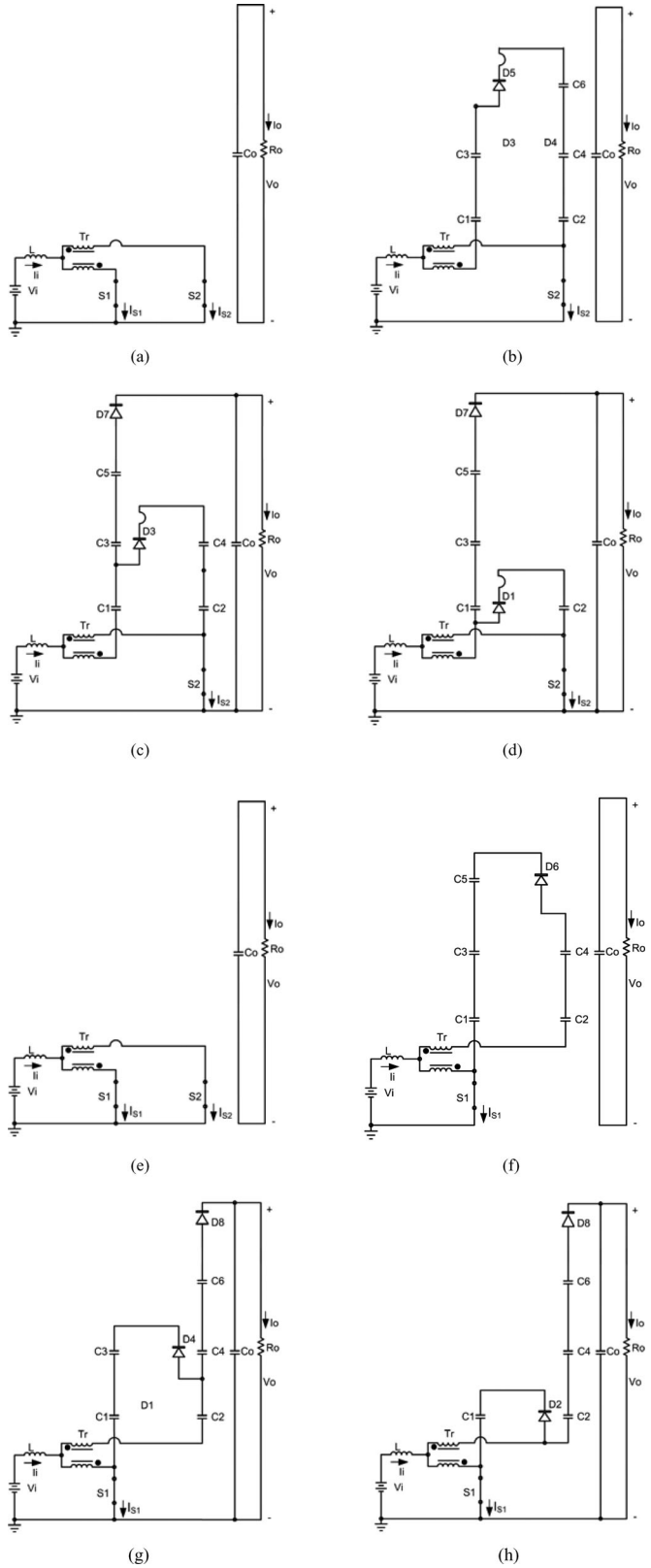

Fig. 4. Operating stages: (a) first stage, (b) second stage, (c) third stage, (d) fourth stage, (e) fifth stage, (f) sixth stage, (g) seventh stage, and (h) eighth stage.

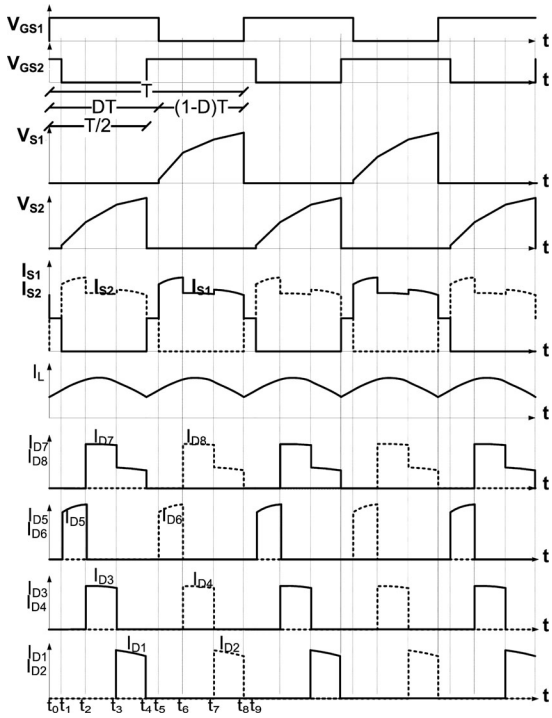

Fig. 5. Main theoretical waveforms.

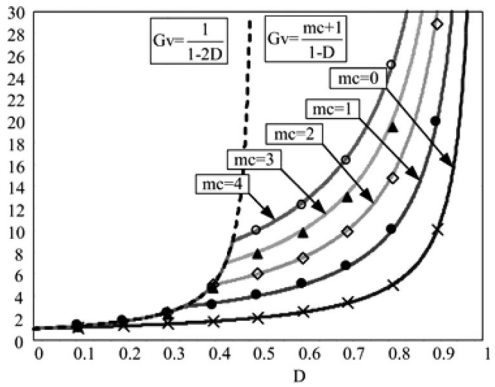

Fig. 6. Static gain curves.

original topology, as seen in Fig. 3. Increased conduction and switching losses are also of major concern in this case.

Even though a simpler arrangement with two VMCs could be considered instead, a design example of the proposed 3SSC boost converter with three cells is presented as follows. It will be also shown that the converter achieves high efficiency over a wide load range.

The specifications are listed in Table I and were used in the implementation of an experimental prototype. Some important calculations are performed in order to evidence the loss mechanism. It is also worth to mention that both conduction and commutation losses are estimated under the rated load condition.

TABLE I
DESIGN SPECIFICATIONS

Parameter	Specification
Rated output power	P_o=1000 W
Minimum input voltage	$V_{i(min)}$=42 V
Maximum input voltage	$V_{i(max)}$=54 V
Rated input voltage	V_i=48 V
Output voltage	V_o=400 V
Number of multiplier cells	mc=3
Switching frequency	f_s=25 kHz
Maximum ripple current through inductor L	ΔI_L=15%·$I_{L(avg)}$
Ripple voltage through multiplier capacitors $C_1 \ldots C_6$	ΔV_{Ck}=8.75%·V_o
Ripple voltage through output capacitor C_o	ΔV_{Co}=1%·V_o
Expected theoretical efficiency	η=95%
Autotransformer turns ratio	a=1

A. Preliminary Calculation

The maximum input power is

$$P_i = \frac{P_o}{\eta} = 1052.3\,\mathrm{W}. \tag{2}$$

The maximum duty cycle is obtained using (3) as follows:

$$D_{\max} = \frac{V_o - V_{i(\min)} \cdot (mc+1)}{V_o} = 0.58. \tag{3}$$

The average and maximum values of the input current are given by (4) and (5), respectively

$$I_{L(\mathrm{avg})} = I_{i(\mathrm{avg})} = \frac{P_o}{V_{i(\min)} \cdot \eta} = 25.06\,\mathrm{A} \tag{4}$$

$$I_{L(\max)} = \frac{P_o}{V_{i(\min)} \cdot \eta} + \frac{\Delta I_L}{2} = 26.94\,\mathrm{A}. \tag{5}$$

B. Inductor

Besides, the normalized ripple current β as a function of the duty cycle is given by

$$\beta = \frac{2 \cdot L \cdot \Delta I_L \cdot f_s}{V_o} = \frac{(1-D)\cdot(2D-1)}{(mc+1)}. \tag{6}$$

Expression (6) is plotted in Fig. 7, where it can be seen that for curve $mc = 3$ and duty cycle $D = 0.75$ the maximum normalized ripple current is β= 0.03125. The respective inductance is calculated from (7) as

$$L = \frac{V_o \cdot \beta}{2 \cdot f_s \cdot \Delta I_L} \cong 70\,\mu\mathrm{H}. \tag{7}$$

The core loss in the inductor is given by [35]

$$P_{L(\mathrm{core})} = \Delta B^{2.4} \cdot \left(K_H \cdot f_L + K_E \cdot f_L^2\right) \cdot V_e = 0.075\,\mathrm{W} \tag{8}$$

where $\Delta B = 0.045$ T is the magnetic flux variation; $K_H = 4\times10^{-5}$ is the hysteresis loss coefficient; $f_L = 2{\cdot}f_s = 50$ kHz is the operating frequency of the inductor; $K_E = 4\times10^{-10}$ is the

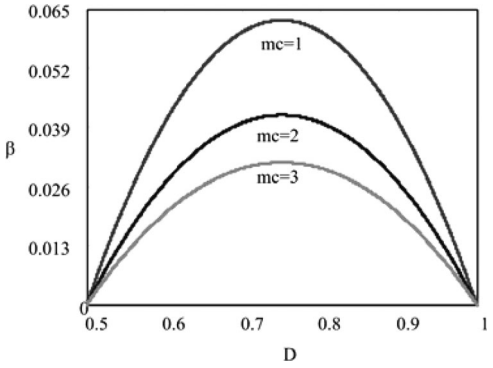

Fig. 7. Normalized ripple current as a function of the duty cycle.

eddy-current loss coefficient; and $V_e = 42.50\,\text{cm}^3$ is the volume of Thornton core NEE-55/28/21.

The copper loss in the inductor is

$$P_{L(\text{copper})} = \frac{\rho \cdot l_t \cdot N_L \cdot I_{L(\text{rms})}^2}{n_L \cdot S_f} = 2.89\,\text{W} \tag{9}$$

where $\rho = 2.078\times10^{-6}\ \Omega\cdot\text{cm}$ is the copper resistivity at 70 °C; $l_t = 11.6$ cm is the average length of one turn; $N_L = 15$ is the number of turns of the inductor; $I_{L\,(\text{rms})} = 25.06$ A is the rms current through the inductor; $n_L = 62$ is the number of wires in parallel; $S_f = 0.001287\ \text{cm}^2$ is the cross-sectional area of copper wire AWG26.

C. Autotransformer

The active power processed by the high-frequency autotransformer is obtained similarly to that processed by its low-frequency counterpart, as demonstrated in [34]. Besides, it has been shown that it corresponds to half of the total output power. The design procedure of such a magnetic element is analogous to that for the transformer of a conventional full-bridge converter [35], i.e.,

$$A_e A_w = \frac{P_i/2}{K_T \cdot K_U \cdot K_P \cdot J_{\max} \cdot \Delta B_{\max} \cdot 2 \cdot f_s} \cdot 10^4 = 12.22\,\text{cm}^4 \tag{10}$$

where A_eA_w is the core area product; $K_T = 1$ is the topology factor; $K_U = 0.4$ is the window utilization factor; $K_P = 0.41$ is the primary winding utilization factor; $J_{\max} = 350\ \text{A/cm}^2$ is the magnetic flux density; $\Delta B_{\max} = 0.15$ is the maximum magnetic flux variation; and $f_s = 25$ kHz is the operating frequency of the transformer.

Core NEE-65/33/26 manufactured by Thornton is then chosen, whose characteristics are as follows: $A_e = 5.32\ \text{cm}^2$ is the effective core cross-sectional area; $A_w = 3.7\ \text{cm}^2$ is the window area considering the former coil; $A_eA_w = 19.68\ \text{cm}^4$; and $V_E = 78.2\ \text{cm}^3$ is the core volume.

The number of turns for the autotransformer windings is

$$N_T = \frac{V_{i\,\min}}{2 \cdot (1 - D_{\max}) \cdot A_e \cdot \Delta B_{\max} \cdot 2 \cdot f_s} \cdot 10^4 \geq 12.53\,\text{turns}. \tag{11}$$

Considering the presence of the skin effect, the maximum diameter of the conductor used in the windings must be lower than [36]

$$d_f = 2 \cdot \frac{6.62}{\sqrt{f_s}} = 2 \cdot \frac{6.62}{\sqrt{25\times10^3}} = 0.084\,\text{cm}. \tag{12}$$

The core loss in the autotransformer is given by

$$P_{T(\text{core})} = \Delta B^{2.4} \cdot \left(K_H \cdot f_T + K_E \cdot f_T^2\right) \cdot V_E = 2.4714\,\text{W} \tag{13}$$

where $\Delta B = 0.15$ is the magnetic flux variation; $K_H = 4\times10^{-5}$ is the hysteresis loss coefficient; $K_E = 4\times10^{-10}$ is the eddy-current loss coefficient; and $V_e = 78.2\ \text{cm}^3$ is the core volume.

The copper loss in the windings of the transformer is

$$P_{T(\text{copper})} = \frac{2 \cdot \rho \cdot l_T \cdot N_T \cdot I_{T(\text{rms})}^2}{n_T \cdot S_f} = 4.90\,\text{W} \tag{14}$$

where $\rho = 2.078\times10^{-6}\ \Omega\cdot\text{cm}$ is the copper resistivity at 70 °C; $l_T = 14.24$ cm is the average length of one turn; $n_T = 28$ is the number of wires in parallel; $S_f = 0.001287\ \text{cm}^2$ is the cross-sectional area of copper wire AWG26; and $N_T = 19$ is the number of turns.

D. Capacitors

The multiplier capacitors C_n and the output capacitor C_o can be obtained from the following expressions:

$$C_n = C_{n+1} = \frac{(mc - n + 1)}{8} \frac{I_{i(\text{avg})} \cdot (1 - D_{\max})}{f_s \cdot \Delta V_{Ck}}$$

for $n = 1, 2, 3,$ and $mc = 3$

$$C_1 = C_2 \cong 4.5\,\mu\text{F} \quad C_3 = C_4 \cong 3.0\,\mu\text{F}$$
$$C_5 = C_6 \cong 1.5\,\mu\text{F} \tag{15}$$

$$C_o \cong \frac{I_o \cdot (2D_{\max} - 1)}{\Delta V_{Co} \cdot 2 \cdot f_s} \cong 2\,\mu\text{F for pure resistive load.} \tag{16}$$

In standalone applications, an inverter is typically connected to the output of the high-gain dc–dc converter. Considering this type of application, a 470 μF/450 V capacitance was adopted for the filter capacitor C_o.

E. Main Switches

The maximum voltage across the main switches S_1 and S_2, diodes D_7 and D_8, and multiplier capacitors $C_1 \ldots C_6$ is given by (17) which is valid when the ripple voltage across the capacitors is neglected:

$$V_{S1-S2} = V_{C1-C6} = V_{D7-D8} = \frac{V_{i(\min)}}{(1 - D_{\max})} = 114.28\,\text{V}. \tag{17}$$

The average current and the rms current through the switches are given by (18) and (19), respectively

$$I_{S1(\text{avg})} = I_{S2(\text{avg})} = \frac{1}{8} \cdot (D_{\max} + 3) I_{L(\max)} = 11.21\,\text{A} \tag{18}$$

$$I_{S1(\mathrm{rms})} = I_{S2(\mathrm{rms})} = \frac{I_{L(\max)}}{24}\cdot\sqrt{3\,(101 - 53D_{\max})} = 15.16\,\mathrm{A}. \quad (19)$$

MOSFET IRFP4227 is then chosen as the main switch, whose characteristics are as follows: drain to source voltage $V_{DS} =$ 200 V; diode forward voltage $V_{(F)} = 1.3$ V; drain current $I_D =$ 46 A at $T_c = 100$ °C; on resistance $R_{DS(\mathrm{on})} = 37.9$ mΩ at T_j = 100 °C; rise time $t_r = 20$ ns; fall time $t_f = 31$ ns.

The conduction loss regarding each main switch is obtained from

$$P_{S1\ldots S2(\mathrm{cond.})} = R_{DS(\mathrm{on})}\cdot I^2_{S1(\mathrm{rms})} = 8.71\,\mathrm{W}. \quad (20)$$

The switching loss during turn ON and turn OFF for a single switch is

$$P_{S1\ldots S2(\mathrm{sw.})} = \frac{f_s}{2}\cdot(t_r + t_f)\cdot I_{S1(\mathrm{avg})}\cdot V_{S1} = 0.837\,\mathrm{W}. \quad (21)$$

F. Diodes

The maximum peak reverse voltage (PIV) across diodes D_7 and D_8 is given by (17). On the other hand, the maximum peak reverse voltage across diodes $D_1 \ldots D_6$ is obtained from

$$V_{D1-D6} = 2\cdot V_{D7-D8} = 228.571\,\mathrm{V}. \quad (22)$$

The average currents through diodes $D_1 \ldots D_8$ are given as

$$I_{D1\ldots D8(\mathrm{avg})} = \frac{I_o}{2} = 1.25\,\mathrm{A} \quad (23)$$

Ultrafast diode MUR460 is then chosen, whose characteristics are as follows: reverse voltage $V_{D(\mathrm{rev.})} = 600$ V; forward voltage $V_{D(F)} = 1.28$ V; average forward current $I_F = 4$ A; reverse recovery time $t_{\mathrm{rr}} = 50$ ns.

The estimated conduction losses regarding each diode are

$$P_{D1(\mathrm{cond.})-D8(\mathrm{cond.})} \cong V_{D(F)}\cdot I_{D1(\mathrm{avg})} \cong 1.6\,\mathrm{W}. \quad (24)$$

Switching losses regarding the diodes are given by

$$P_{D1\ldots D6(\mathrm{sw.})} = \frac{1}{2}\left(V_{D(F)P} - V_{D(F)}\right) I_{D1(\mathrm{avg})} t_{\mathrm{rise}} f_s + V_{D1} Q_{\mathrm{rr}} f_s = 0.572\,\mathrm{W} \quad (25)$$

$$P_{D7\ldots D8(\mathrm{sw.})} = \frac{1}{2}\left(V_{D(F)P} - V_{D(F)}\right) I_{D7(\mathrm{avg})} t_{\mathrm{rise}} f_s + V_{D7} Q_{\mathrm{rr}} f_s = 0.286\,\mathrm{W} \quad (26)$$

where $V_{D(F)P} = 1.5$ V is the maximum value assumed by the forward voltage, $t_{\mathrm{rise}} = 18$ ns is the rise time of the current through the diode, and $Q_{\mathrm{rr}} = 100$ nC is the amount of charge stored in the intrinsic capacitance of the diode.

The estimated total loss of the converter is

$$P_{\mathrm{total}} = P_{Lb(\mathrm{core})} + P_{L(\mathrm{copper})} + P_{T(\mathrm{core})} + P_{T(\mathrm{copper})} + 2\cdot P_{S1\ldots S2(\mathrm{cond.})} + 2\cdot P_{S1\ldots S2(\mathrm{sw.})} + 8\cdot P_{D1\ldots D8(\mathrm{cond.})} + 6\cdot P_{D1\ldots D6(\mathrm{sw.})} + 2\cdot P_{D7\ldots D8(\mathrm{sw.})} = 46.234\,\mathrm{W}. \quad (27)$$

TABLE II
PROTOTYPE SPECIFICATIONS

Component	Specifications
Inductor L	Core: Thornton NEE 55/28/21 Inductance: 70 µH Number of turns: 15 (62x26AWG) Gap: 1mm
Autotransformer T_r	Core: Thornton NEE-65/33/26 Primary turns: 19 Primary winding: 28×AWG26 Secondary turns: 19 Secondary winding: 28×AWG26
Switches S_1 and S_2	MOSFET IRFP4227
Diodes $D_1 \ldots D_8$	Ultra fast diode MUR460
Capacitors C_1 and C_2	Epcos B32594, 2×2.2 µF / 400 V
Capacitors C_3 and C_4	Epcos B32594, 1 µF +2.2 µF / 400 V
Capacitor C_5 and C_6	Epcos B32594, 2.2 µF / 400 V
Output capacitor C_o	Epcos B43304, 470 µF / 450 V

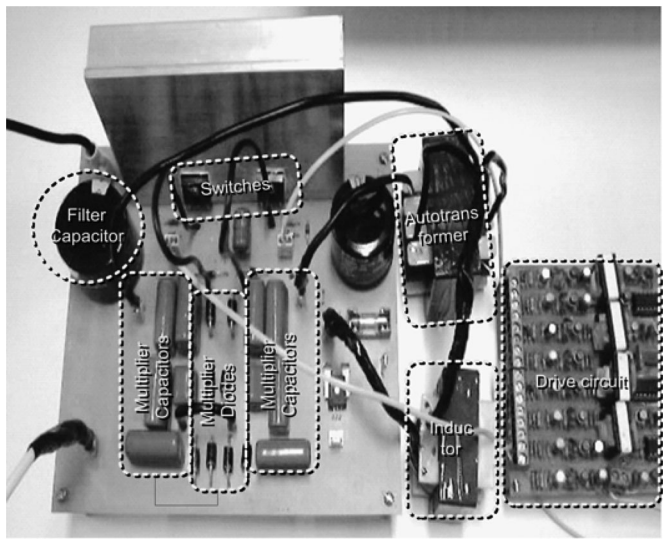

Fig. 8. Photograph representing the experimental prototype.

Therefore, the estimated theoretical efficiency under the rated load condition is obtained from

$$\eta_{\mathrm{theor.}} = \frac{P_o}{P_o + P_{\mathrm{total}}}\cdot 100 \cong 95.58\%. \quad (28)$$

IV. EXPERIMENTAL RESULTS

An experimental prototype for the structure with three multiplier cells has been designed according to the previous guidelines and implemented in laboratory. The components used in the prototype are listed in Table II and a picture is shown in Fig. 8.

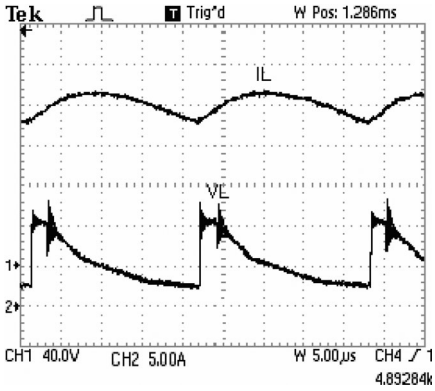

Fig. 9. Current and voltage waveforms for inductor L: (CH1) 40 V/div, 5 μs/div; (CH2) 5 A/div, 5 μs/div.

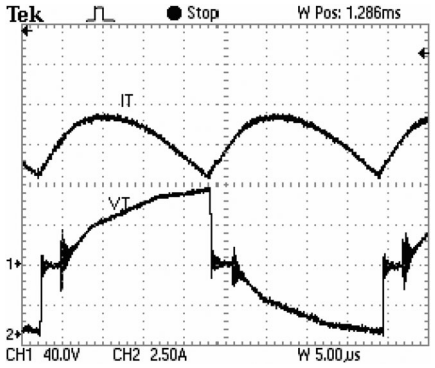

Fig. 10. Current and voltage waveforms for the primary winding of the autotransformer: (CH1) 40 V/div, 5 μs/div; (CH2) 2.5 A/div, 5 μs/div.

Fig. 9 shows the waveforms regarding inductor L, where it can be seen that the ripple current is 6 A. The voltage across the inductor varies from -22 to $+42$ V in Fig. 9.

The voltage and current stresses regarding the autotransformer windings are similar because the number of turns is exactly the same. Therefore, current is equally shared in two halves of the current through inductor L. The ripple current in Fig. 10 is approximately 3.5 A. The peak voltage across each winding is equal to half that across the switch and varies from -76 to $+76$ V. Besides, the average voltage across each winding is null.

Fig. 11 represents the commutation of switches S_1 and S_2. The voltages across the switches are approximately the same, although 180° displaced. The maximum voltage across the switches is 140 V, which is very close to the theoretical calculation. It can be seen that the voltage across the switch is lower at the beginning of the turning-off process. The current through switch S_1 is discontinuous due to the commutation of the multiplier diodes, as predicted in the theoretical analysis. Besides, the current peak is equal to the inductor current, i.e., 30 A.

Fig. 12 presents the voltages across the multiplier diodes D_1, D_3, D_5, and D_7. The voltages across diodes D_1, D_3, and D_5 vary from 200 to 250 V due to the presence of adjacent capacitors. On the other hand, the voltage across diode D_7 is about 140 V due to the absence of such components. Due to the voltage ripple

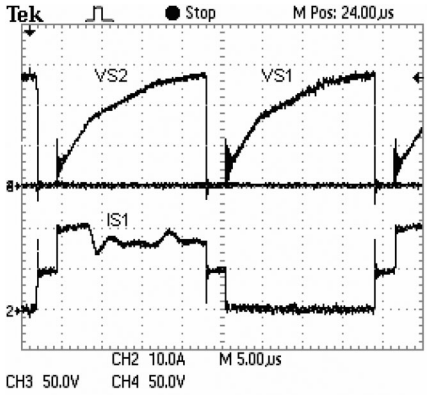

Fig. 11. Voltage across switches S_1 and S_2, and current through switch S_1: (CH3)(CH4) 50 V/div, 5 μs/div; (CH2) 10 A/div, 5 μs/div.

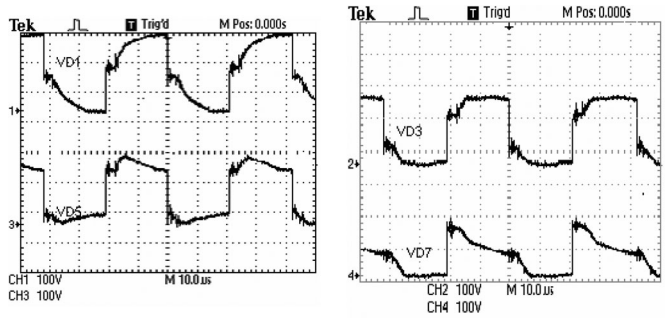

Fig. 12. Voltage waveforms across multiplier diodes: (CH1)(CH3) 100 V/div, 10 μs/div.

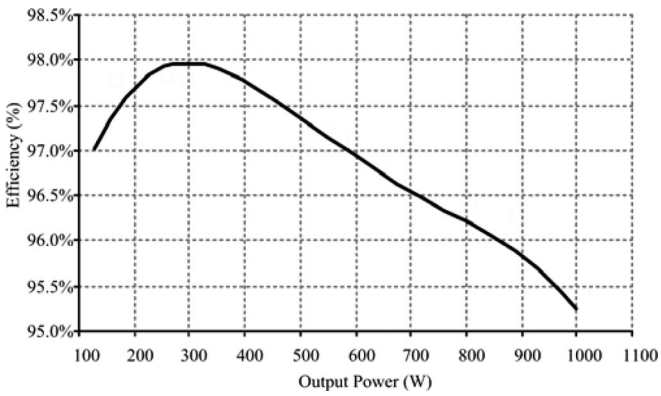

Fig. 13. Efficiency as a function of the output power.

across the capacitors, experimental waveforms show that the maximum voltages across all diodes are less than that predicted in expressions (14) and (19).

Finally, the efficiency curve of the topology designed and implemented according to Tables I and II is depicted in Fig. 13. Maximum efficiency regarding the converter is 97.9%, while good performance is also verified for the entire load range. For instance, efficiency is 95.3% at rated load.

V. Conclusion

This paper has proposed six generalized nonisolated high-gain voltage dc–dc converters. To verify the principle operation of the generated structures, the boost converter was chosen. The topology is adequate for several applications such as photovoltaic systems, fuel cell systems, and UPSs, where high voltage gain between the input and output voltages is demanded.

An important characteristic that can be seen in the experimental results is the reduced blocking voltages across the controlled switches compared to similar circuits, allowing the utilization of MOSFETs with reduced on-resistance. Besides, the advantages of the 3SSC are also incorporated into the resulting topology, e.g., the current is distributed among the semiconductors. Furthermore, only part of the energy from the input source flows through the active switches, while the remaining part is directly transferred to the load without being processed by these switches, i.e., this energy is delivered to the load through passive components, such as the diodes and the transformer windings.

The qualitative analysis, theoretical analysis, losses modeling, and experimental results for a 1-kW prototype have been discussed. The converter achieves about 95.3% efficiency at rated load if compared to similar configurations that were previously proposed in the literature. It is also expected that nonisolated converters based on the 3SSC and VMC may be competitive solutions for high-current-high-voltage-step-up applications if compared with some other isolated approaches.

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