

# Multilevel Inverter Topologies for Stand-Alone PV Systems

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**Abstract**—This paper shows that versatile stand-alone photovoltaic (PV) systems still demand on at least one battery inverter with improved characteristics of robustness and efficiency, which can be achieved using multilevel topologies. A compilation of the most common topologies of multilevel converters is presented, and it shows which ones are best suitable to implement inverters for stand-alone applications in the range of a few kilowatts. As an example, a prototype of 3 kVA was implemented, and peak efficiency of 96.0% was achieved.

**Index Terms**—Multilevel inverter, renewable energy (RE), stand-alone photovoltaic (PV) system.

## I. INTRODUCTION

MULTILEVEL converters have been mainly used in medium- or high-power system applications, such as static reactive power compensation and adjustable-speed drives. In these applications, due to the limitations of the currently available power semiconductor technology, a multilevel concept is usually a unique alternative because it is based on low-frequency switching and provides voltage and/or current sharing between the power semiconductors [1]–[4].

On the other hand, for low-power systems (< 10 kW), multilevel converters have been competing with high-frequency pulsewidth-modulation converters in applications where high efficiency is of major importance. Moreover, lower prices of power switches and new semiconductor technologies, as well as the current demand on high-performance inverters required by renewable energy systems (RES), have extended the applications of multilevel converters [5]–[10].

For the particular case of stand-alone RES (SARES), it is of common sense that it should be capable of supplying alternating current (ac) electricity [11], thus providing compatibility with standard appliances that are cheap and widely available. In addition, due the intermittent nature of almost all renewable energy (RE) sources, most single-consumer SARES include an energy storage device that is usually implemented by lead-acid battery banks [12]–[14].

Manuscript received September 30, 2007; revised March 7, 2008. This work was supported by the University of Kassel.

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Digital Object Identifier 10.1109/TIE.2008.922601

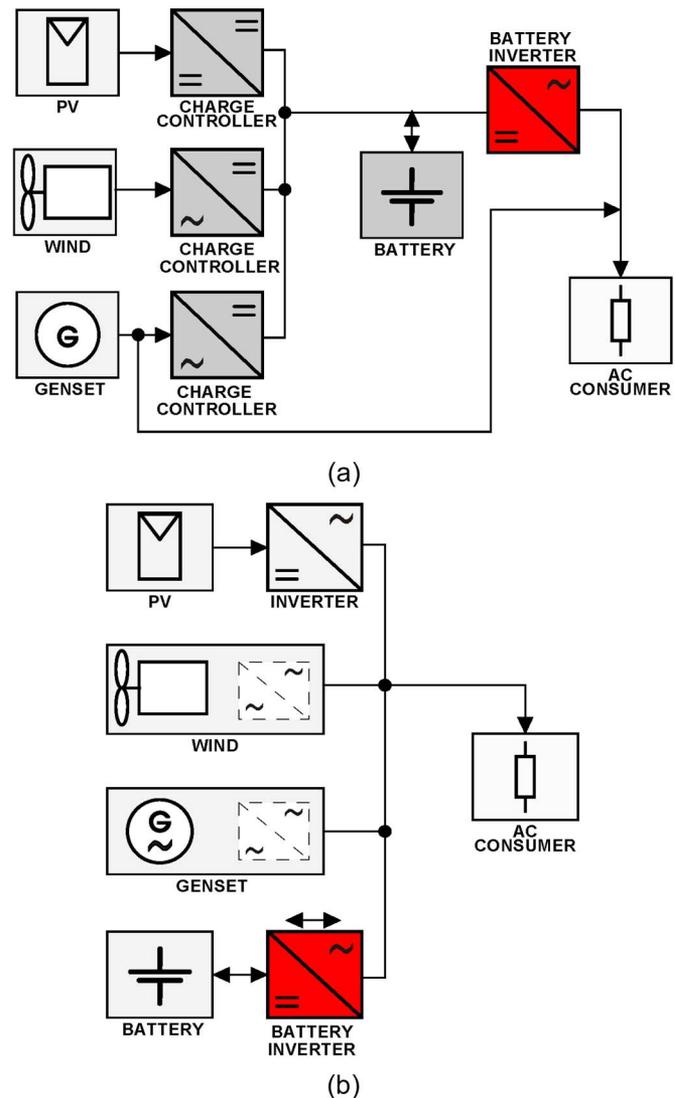


Fig. 1. Modular hybrid systems. (a) DC-bus modular system. (b) AC-bus modular system.

According to these facts, it is evident that a device capable of converting a single dc voltage from a battery bank into an ac voltage is a key element of most stand-alone photovoltaic (PV) systems. These dc/ac converters, which are commonly referred to as inverters, have experienced great evolution in the last decade due to their wide use in uninterruptible power supplies and industrial applications. However, it is still a critical component to most SARES, and the development of high-performance inverters is a challenge even today [15]–[17].

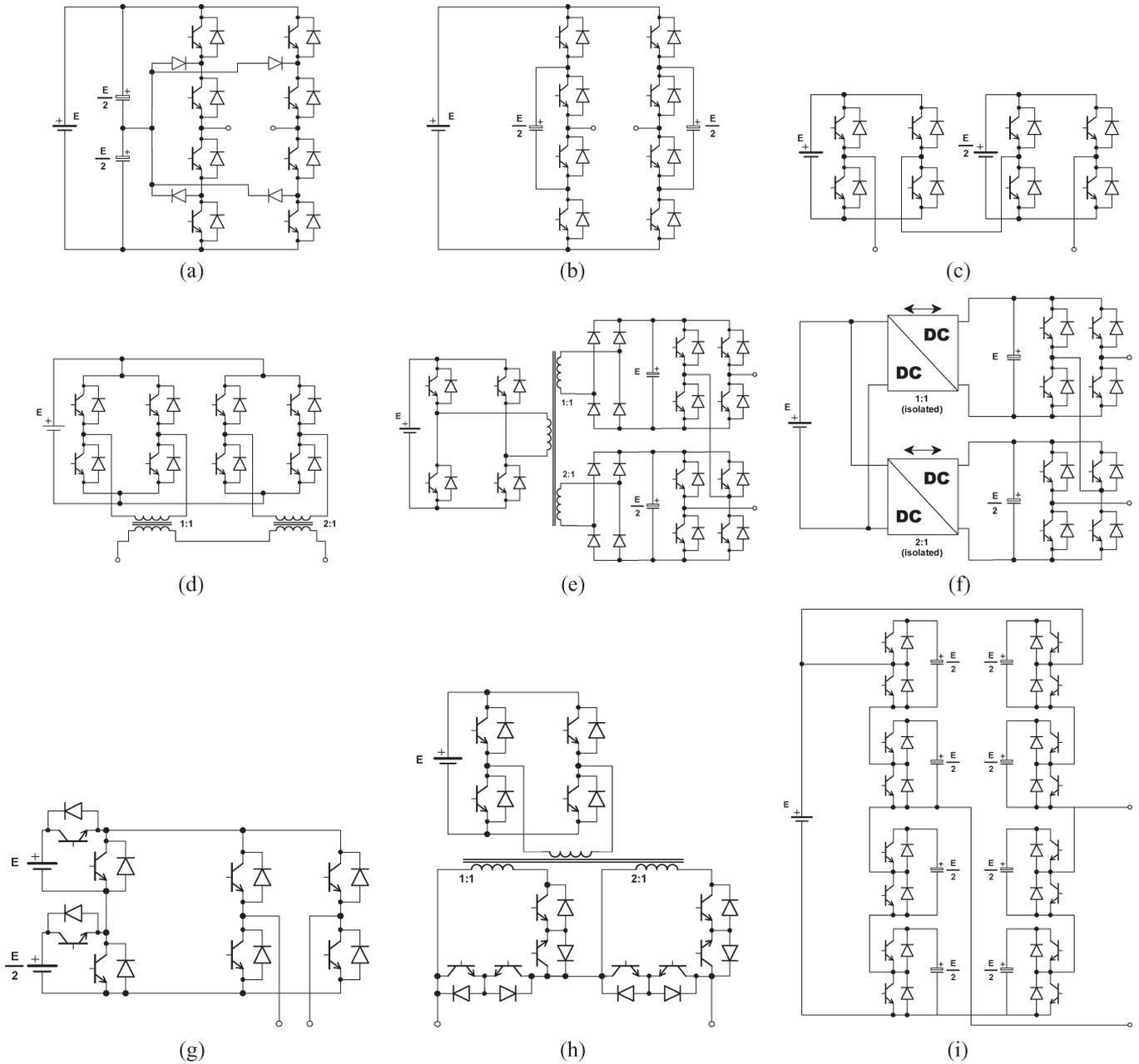


Fig. 2. Multilevel inverter topologies. (a) NPC. (b) Flying capacitors. (c) Cascade H-bridge. (d) Multiple transformer. (e) and (f) Variations of the cascade H-bridge. (g) Multiple source. (h) Multiwinding transformer. (i) Modular topology.

Most of the small SARES for rural electrification present configurations that are variations of the complex hybrid systems that are presented in Fig. 1.

In both dc- and ac-bus configurations, since the generator does not continuously operate and considering the intermittency of the RE sources, it is possible to conclude that the battery inverter should be designed to fully support the loads at some time periods. Therefore, independently of the system configuration, it is possible to identify that at least one “strong battery inverter” is required.

Having in mind that SARES only make sense if they can be reliable and flexible, then all balance-of-system components must be accomplished with these characteristics. This way, to the best of the author’s knowledge, the most important

characteristics of a RES battery inverter, concerning the order of importance, are as follows:

- 1) reliability (most important);
- 2) surge power capacity;
- 3) no-load consumption and efficiency.

This paper investigates which multilevel topologies better meet the current demand on high-performance battery inverters for stand-alone PV system applications.

## II. COMPILATION OF TOPOLOGIES

In this section, short reviews of the most common topologies are presented. Fig. 2 shows the topologies considered in this paper.

TABLE I  
SPECIFICATIONS FOR DEFINING A HIGH-PERFORMANCE BATTERY INVERTER

Id.	Inverter characteristic	Priority
M1	<b>Single source input</b> <i>Justification: Required by standard designs.</i>	<b>Mandatory</b>
M2	<b>Mainly based on low-frequency switching</b> <i>Justification: Maximum robustness and efficiency can be achieved by using low-frequency switching.</i>	<b>Mandatory</b>
M3	<b>Capable to feed loads with DC level component</b> <i>Justification: Like the grid, it is desired that SARES must be capable to support loads of diverse nature.</i>	<b>Mandatory</b>
M4	<b>Suitable to implement high-resolution waveform</b> <i>Justification: The use of filters for low-frequency waveforms is not practical for these applications.</i>	<b>Mandatory</b>
A1	<b>Bi-directional (4-quadrant operation)</b> <i>Justification: Improve robustness. (It is optional because a battery charger can be added).</i>	<b>Optional</b>
A2	<b>Input-output isolation</b> <i>Justification: Assures more flexibility.</i>	<b>Optional</b>

A. Diode-Clamped Topology

Fig. 2(a) shows a three-level neutral-point-clamped (NPC) inverter, as proposed by Nabae *et al.* [18]. It was the first widely popular multilevel topology, and it continues to be extensively used in industrial applications. Later, the NPC inverter was generalized for a greater number of levels, using the same concept of diode-clamped voltage levels, which resulted in the current designation of a diode-clamped converter [19].

As it can be seen in Fig. 2(a), the three-level NPC inverter uses capacitors to generate an intermediate voltage level, and the voltages across the switches are only half of the dc input voltage. Due to capacitor voltage balancing issues, practical diode-clamped inverters have been mostly limited to the original three-level structure.

B. Flying Capacitor

The three-level flying capacitor topology, as shown in Fig. 2(b), can be considered as a good alternative to overcome some of the NPC topology drawbacks [20], [21]. In this topology, additional levels and voltage clamping are achieved by means of capacitors that “float” with respect to the dc source reference. It does not require additional clamping diodes and provides redundant switch states that can be used to control the capacitor charge even under loads with the dc level [22]. Nevertheless, larger structures require a relatively high number of capacitors, and additional circuits are also required to initialize the capacitor charge.

C. Cascade H-Bridge

This topology is composed of several H-bridge converters in cascade connection. Fig. 2(c) shows a two-cell inverter.

The cascade topology allows the use of dc sources with different voltage values, and high-resolution multilevel waveforms can be achieved with a relatively low number of components [23]–[27]. In addition, dc sources can be added or subtracted, which can increase the number of output levels.

TABLE II  
SUMMARY OF THE CHARACTERISTICS OF THE MOST COMMON MULTILEVEL TOPOLOGIES

Topology	M1	M2	M3	M4	A1	A2
Diode clamped	Y	Y	N	N	Y	N
Flying capacitor	Y	Y	Y	N	Y	N
H-bridge (isolated DC sources)	N	Y	Y	Y	Y	N
<b>H-bridge (multi-winding transf.)</b>	Y	Y	Y	Y	N	Y
H-bridge (+ isolated DC/DC conv.)	Y	N	Y	Y	Y	Y
<b>Multiple transformer</b>	Y	Y	Y	Y	Y	Y
Multiple source	N	Y	Y	Y	Y	Y
<b>Multi-winding transformer</b>	Y	Y	Y	Y	Y	Y
Modular	Y	Y	N	Y	Y	N

Y: Characteristic is available ; N: not available

TABLE III  
DESIGN DATA AND EXPECTED PERFORMANCE FOR SELECTED TOPOLOGIES

	Fig. 2(e)	Fig. 2(d) / 3-cell	Fig. 2(d) / 4-cell	Fig. 2(h)
Number of cells	4	3	4	4
Maximum p	15	13	15	15
Transformers	1	3	4	1
Power switches	20	12	16	20
Capacitors	4	0	0	0
Diodes	16	0	0	0
Isolated drivers	8	0	0	8
Reliability	Medium	High	High	High
Surge Power	High	High	High	High
Efficiency	Medium	Medium	Medium	High
No-load Power	Medium	Medium	Medium	Medium
Competitiveness	Medium	High	Medium	Medium

\* Using topologies capable to produce at least 12 steps per quarter cycle.

Although the original cascaded topology requires several isolated dc sources, in some systems, they may be available through batteries or PV panels; thus, it has been used to implement high-efficiency transformerless inverters [30], [32].

D. Multiple Transformer

Fig. 2(d) shows a multiple-transformer topology composed of two cells. It is similar to the cascaded H-bridge topology, but the outputs of the isolation transformers are cascaded instead of directly cascading the H-bridge outputs. As a result, only one dc source is required.

Currently, there are commercial inverters (for SARES applications) in the market that are based on this topology [28], [29]. In practice, these inverters have been proved to be robust and reliable. One disadvantage of this topology is the fact that it requires several low-frequency transformers.

E. Other Variations of the Cascade H-Bridge

If only one dc source is available, then it is possible to use the topology shown in Fig. 2(e) [31]. This topology is simple, but losses in additional rectifier diodes can be significant, and it does not support a bidirectional power flow. The topology shown in Fig. 2(f) can be very efficient if soft-switching dc/dc converters are used [6]. On the other hand, this topology is based on high-frequency switching, and inherent benefits of low-frequency switching are lost.

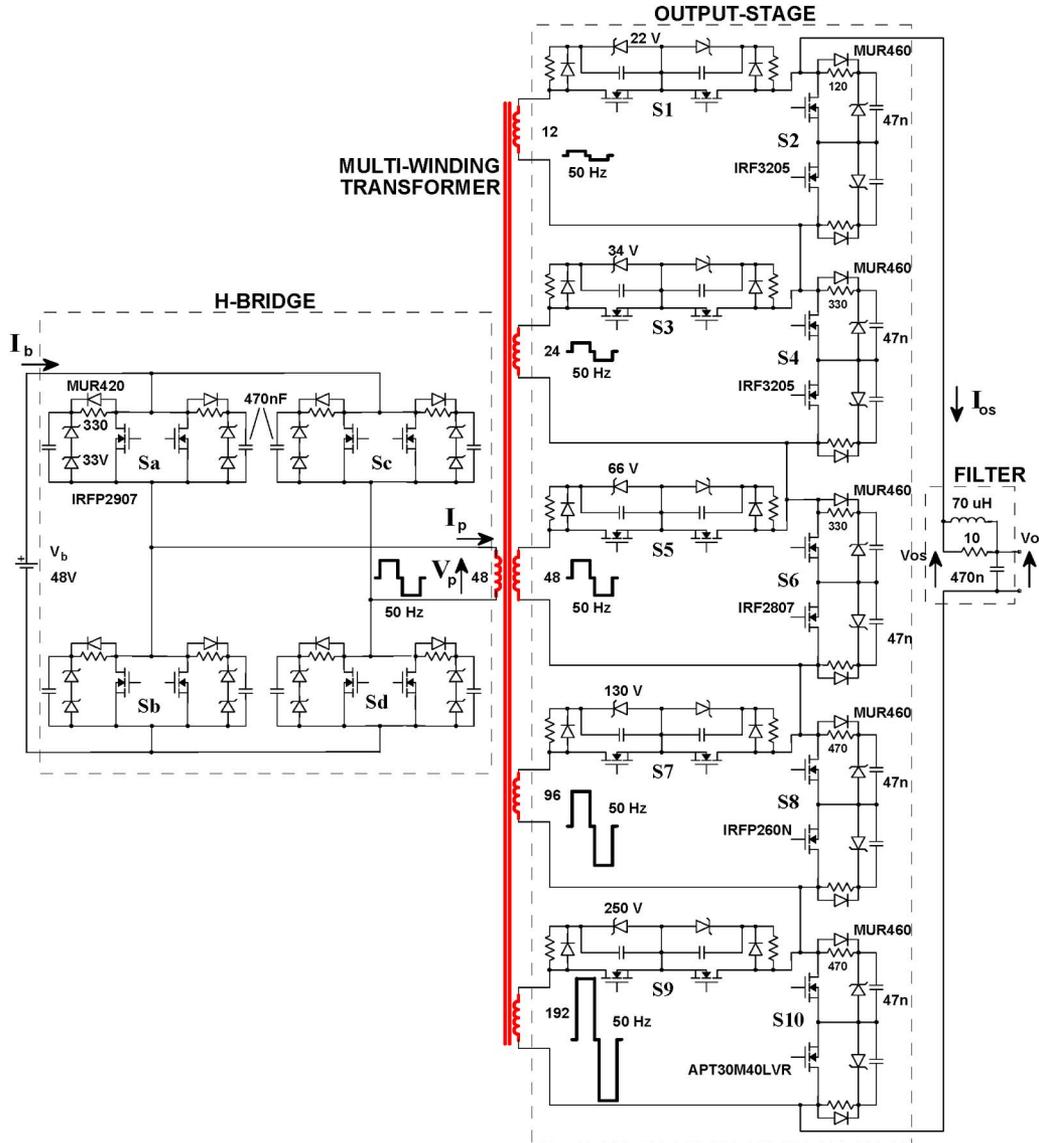


Fig. 3. Schematic of the power structure of the proposed inverter.

F. Multiple Source

The multiple-source topology, as shown in Fig. 2(g), uses several isolated dc sources to produce a rectified multilevel waveform, which is then converted into an ac voltage [33], [34].

In practice, the multiple-source topology is one of the most efficient multilevel topologies currently available. It has been tested in some RES for more than ten years, and it has proved to be very efficient, robust, and reliable [35]. The disadvantage of this topology is the fact that it requires several isolated dc sources and does not provide input–output isolation.

G. Multiwinding Transformer

The multiwinding-transformer topology can be considered as a variation of the multiple-source topology. A three-cell multiwinding inverter is shown in Fig. 2(h).

Unlike the multiple-source topology, the multiwinding topology requires only a single dc input, which is achieved using a multiwinding line-frequency transformer. It provides input–

output isolation, and because it employs only one transformer, high efficiency can be achieved. The major disadvantage is the relatively high number of switches presented in the output stage. Additional information about this topology can be found in [36]–[38].

H. Modular Topology

Fig. 2(i) shows an eight-module modular topology that has been recently proposed for high-power applications [39], [40].

III. TRIAL OF TOPOLOGIES

As discussed, most SARES require a single input battery inverter with improved characteristics of reliability, surge power capability, and efficiency. In addition, such kind of inverter must be capable of working with loads of diverse nature, such as house appliances, and, thus, must produce an output voltage with acceptable waveform quality.

Taking into account these requirements, it is possible to define a list of characteristics required by a high-performance battery inverter, as presented in Table I.

In accordance with Table I, the characteristics of all the topologies shown in Fig. 2 are summarized in Table II.

As it can be seen in Table II, only three topologies meet all mandatory characteristics. While multiple-transformer and multiwinding-transformer topologies meet all the characteristics, the H-bridge (multiwinding transformer) does not support full four-quadrant operation.

Finally, the presented analysis shows that the multiple-transformer and multiwinding-transformer topologies are the most suitable to implement high-performance battery inverters. Table III shows the achieved design data and expected performance for these selected topologies.

It is important to note that evaluation of the expected performance parameters took into account six factors.

- 1) Structures that can produce at least 12 steps per quarter cycle are assumed. This is a practical value that allows an output voltage regulation of approximately 40% (total harmonic distortion (THD)  $\leq 5\%$ ) to be produced with a minimum number of switching transitions [37].
- 2) Reliability of the H-bridge inverter was lowered because of the presence of capacitors (usually electrolytic).
- 3) Efficiency of the H-bridge inverter is limited by the rectifier diodes.
- 4) Efficiency of both multiple-transformer/three-cell and four-cell inverters is limited by the possible reverse power flow, which is a situation that occurs when additional levels are produced by reverting the polarity of one or more cells in respect to the output voltage polarity (subtraction of levels). In addition, several individual transformers are employed, and each one always carries the total current at any instant.
- 5) Conversion efficiency of the multiwinding-transformer inverter is considered high because it uses only one transformer and the load current is shared between transformer output coils and switches.
- 6) Market competitiveness of the multiple-transformer/three-cell inverter is considered high because the additional cost of the three transformers is compensated by the reduced number of power devices and drivers.

The presented analysis shows that the multiple-transformer and multiwinding-transformer topologies are the most suitable to implement high-performance battery inverters. It is also expected that the multiwinding-transformer topology can achieve better efficiency than the multiple-transformer one if same rules and similar components are used in their design.

#### IV. EXAMPLE OF APPLICATION

To validate the proposed analysis, a 63-level inverter of 3 kVA ( $48 V_{dc}/230 V_{ac}/50 \text{ Hz}$ ) was implemented using the multiwinding-transformer topology. Fig. 3 shows the schematic (power structure) for the proposed five-cell inverter.

As it can be seen in Fig. 3, a 48-V battery bank is connected to an H-bridge that switches at 50 Hz and feeds the primary of the multiwinding transformer. The five isolated secondary coils

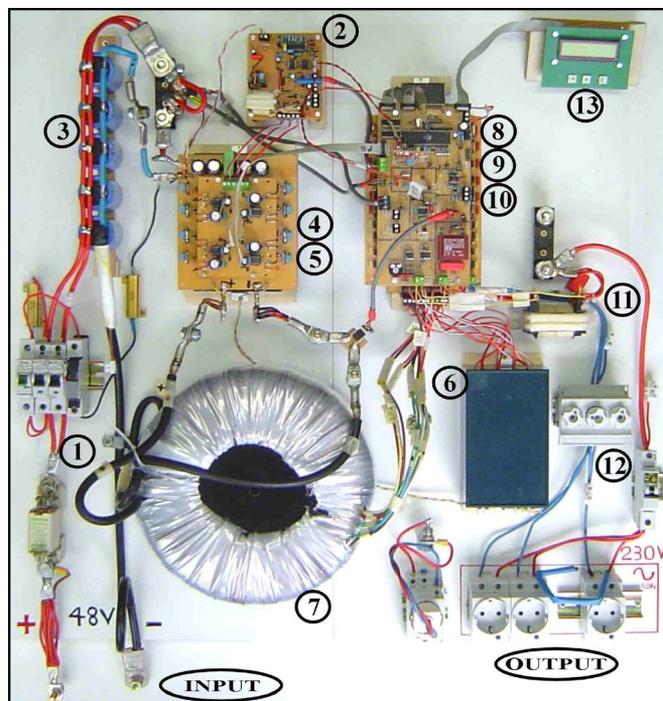


Fig. 4. Prototype top view: (1) input protections; (2) auxiliary power supply; (3) input filter capacitors; (4) and (5) H-bridge and its driver board; (6) auxiliary transformer—ten isolated power supply for output stage drivers; (7) multiwinding transformer; (8) and (9) output stage and its driver board; (10) controller board; (11) output filter; and (12) output protections.

of the transformer are then combined through the output stage (composed of ten ac switches:  $S_1-S_{10}$ ) to produce a staircase waveform. The small filter connected to the output was added to filter the high-frequency spikes generated due to the nonideal switching. The partial output voltages are multiples of two (12 V, 24 V, . . . , 192 V), thus making it possible to produce waveforms with up to 63 levels.

Fig. 4 shows the top view of the experimental setup, which is a full-functional inverter and does not require any external circuits for its operation (except for the batteries). The use of a toroidal transformer made it possible to decrease the no-load losses, thus improving the efficiency at light loads.

The block diagram of the implemented prototype is shown in Fig. 5. The power for the control circuits and H-bridge drivers is supplied by a switch-mode power supply (SMPS) (2), which is connected to the input. The isolated drivers of the output stage switches are fed by an auxiliary low-power transformer, which is connected to the H-bridge output.

The controller is based on an 8-bit AT90S8535 microcontroller (running at 11.0592 MHz) from ATMEL. The control program was developed in C language, and all switch signals were implemented in lookup tables stored in the microcontroller internal memory. According to the battery voltage and output current, it was possible to adjust the output voltage by changing the lookup table. A total of 16 lookup tables were implemented (33, 35, . . . , 63 levels). Fig. 6 shows the driver signals for all switches (a 63-level waveform). These signals were sampled at  $75 \mu\text{s}$ , and a lookup table was built (the same process was used for other number of levels).

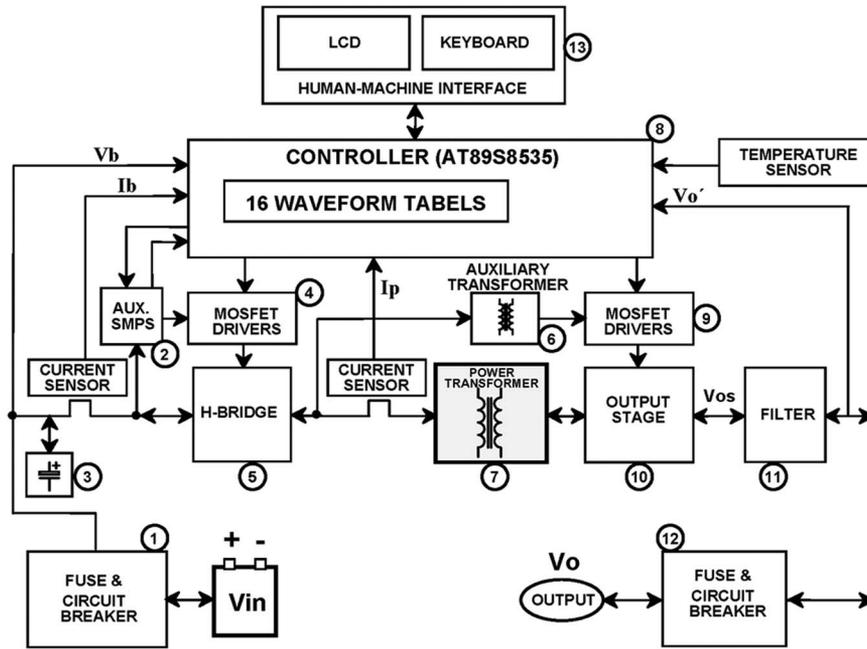


Fig. 5. Block diagram of the implemented prototype.

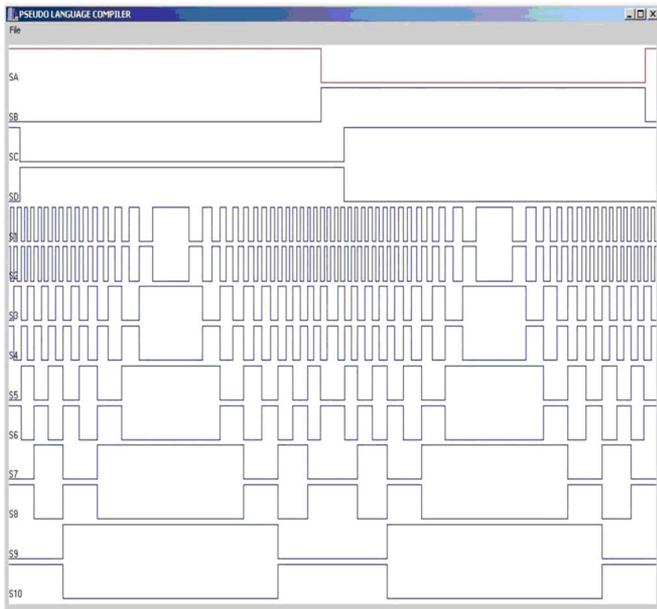


Fig. 6. Driver signals of all switches (63 levels).

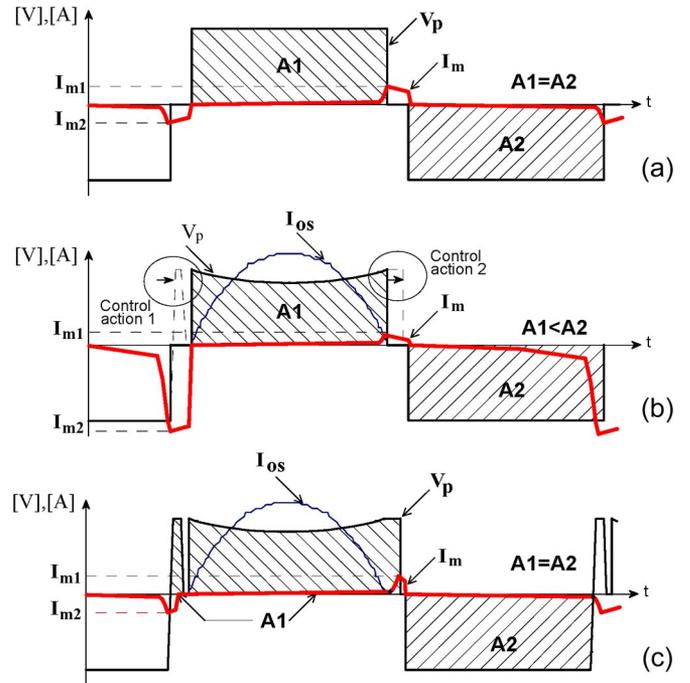


Fig. 7. Illustration of the implemented mechanism to avoid transformer saturation.

Since the proposed inverter is based on a line-frequency transformer, it was fundamental to develop a method to avoid transformer saturation. Fig. 7 illustrates the principle used to implement this control.

As it can be seen in Fig. 7(a), under normal operation condition, the voltage produced by the H-bridge is perfectly balanced (areas A1 and A2 are equal), and the transformer magnetization current  $I_m$  is balanced ( $I_m$  peaks, i.e.,  $I_{m1}$  and  $I_{m2}$ , are equal). On the other hand, if the converter feeds a half-wave load, as shown in Fig. 7(b), then the voltage applied to the transformer presents a dc level ( $A1 < A2$ ) due to the voltage drops in the positive half-cycle. As a consequence, the trans-

former becomes strongly saturated in the negative direction, and  $I_{m2}$  becomes very high. In this case, the proposed control mechanism provides a way to increase the positive half-cycle time period, thus compensating the voltage drop. This control mechanism uses the hold-on-at-zero interval to implement two actions.

Action 1: At the end of the negative half-cycle, a floating time period (all H-bridge switches are turned off) replaces a part of the hold-on-at-zero interval.

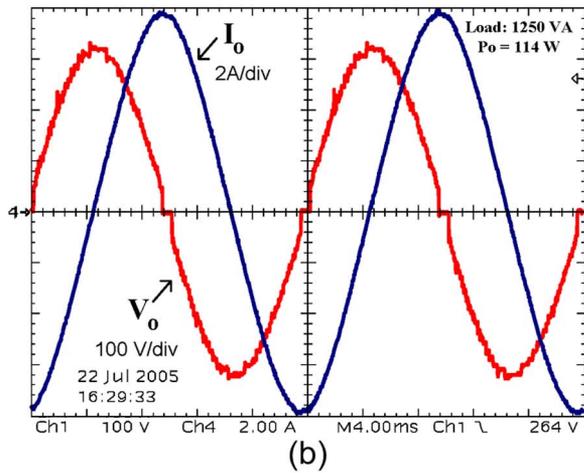
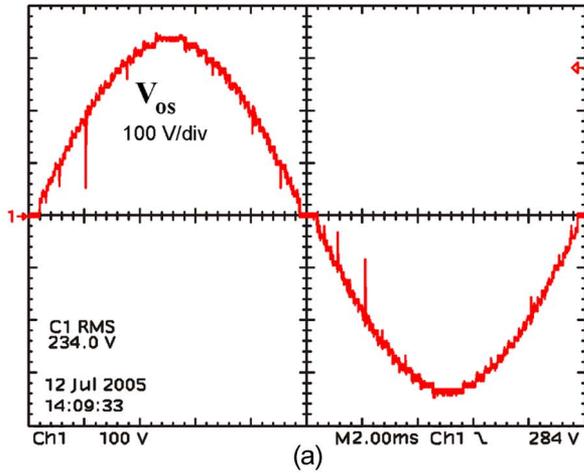


Fig. 8. (a) Output voltage (before filter) at a no-load condition. (b) Waveforms for operation under an inductive load.

Action 2: The end of the positive half-cycle is simply postponed, thus replacing a part of the hold-on-at-zero interval.

The output voltage waveform is shown in Fig. 8(a). Since the proposed structure provides up to 31 levels, the output voltage is adjusted by simply changing the number of levels; thus, no special high-frequency modulation is required. As it can be seen, the experimental output waveform approximates a perfect sinusoidal shape, apart from the distortions near zero crossing. These distortions correspond to a fixed time of 700  $\mu$ s, where the output voltage is forced to be zero and is used to control transformer unbalancing. The THD was lower than 4% for any number of levels between 31 and 63, and the output voltage regulation was implemented by simply changing the output number of levels.

Operation of a nearly pure inductive load is presented in Fig. 8(b), where it is possible to verify that the load current is delayed by almost 90°.

A refrigerator is commonly desired in residential applications, and it is known to be a problem in many small stand-alone systems due to its high startup current. Fig. 9 shows the waveforms acquired at the startup of a refrigerator.

At steady-state operation, the measured current was 1.0 A (root mean square, rms), whereas the current at startup is

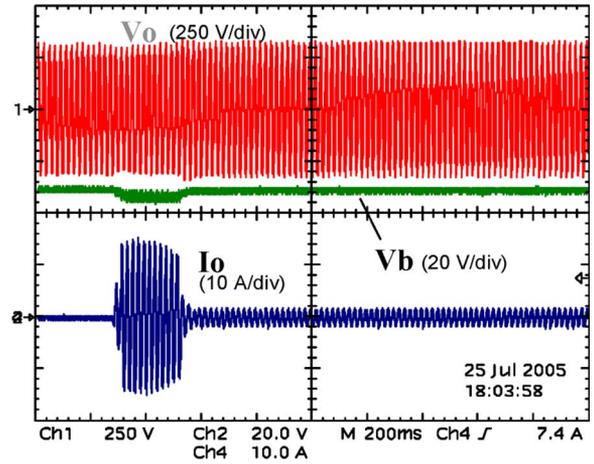


Fig. 9. Waveforms for a refrigerator startup.

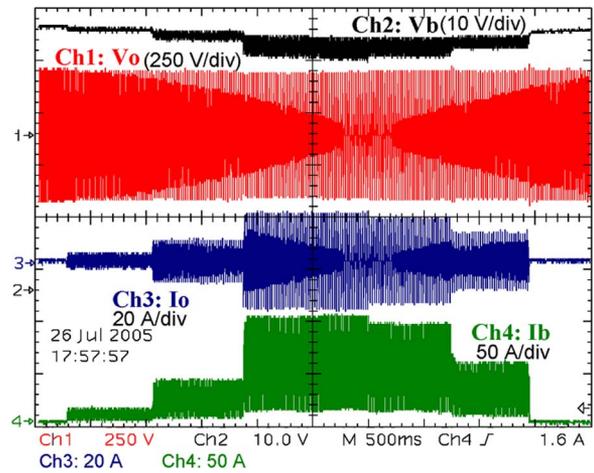


Fig. 10. Sequence of load steps.

approximately 10.6 A (rms). Thus, even this small refrigerator may require 2.4 kVA at startup.

Fig. 10 shows the prototype operation under a sequence of resistive load steps (0 W  $\Rightarrow$  500 W  $\Rightarrow$  1000 W  $\Rightarrow$  3000 W  $\Rightarrow$  2500 W  $\Rightarrow$  1500 W  $\Rightarrow$  0 W). As it can be seen, despite the large changes in the battery bank voltage  $V_b$  and the input and output currents  $I_b$  and  $I_o$ , respectively, the converter was capable of producing a stable output voltage  $V_o$ .

The efficiency versus output power characteristic curves of the implemented prototype are shown in Fig. 11. Peak efficiency of 96.0% at an output power of 945 W was measured for an input voltage of 48 V.

Fig. 12 shows how the no-load losses are internally distributed. It can be seen that the transformer is responsible for most losses, followed by the switching losses in the output stage.

In addition to the presented results, the proposed prototype was also capable of successfully operating with nonlinear loads, such as microcomputers and half-wave loads (up to 1500 W). Due to its bidirectional characteristic and the implemented control to prevent transformer unbalancing, no problems were observed while operating these loads.

A summary of the main characteristics of the prototype and some commercial inverters is shown in Table IV.

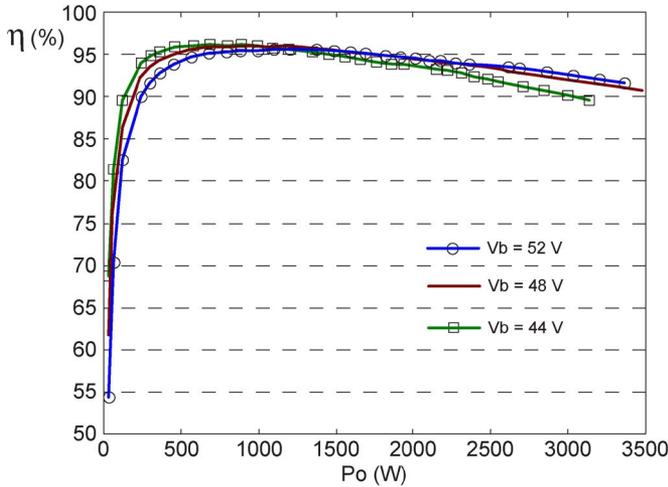


Fig. 11. Efficiency  $\times$  output power characteristic (resistive load).

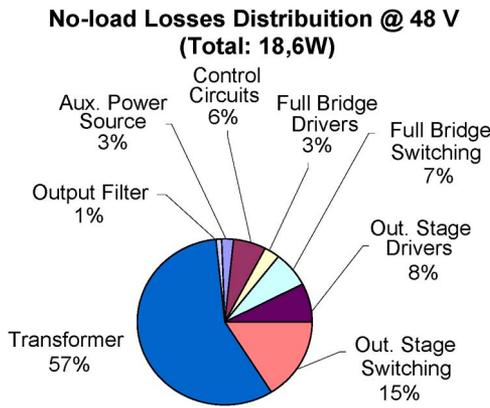


Fig. 12. No-load loss distribution.

TABLE IV  
COMPARISON OF INVERTERS

No.	Inverter	Power (VA)	$\eta_{pk}(\%)$	No-Load (W)
1	<b>Implemented prototype</b>	<b>3000</b>	<b>96.0</b>	<b>18.6</b>
2	Phoenix 48/3000/35	3000	95.0	10.0
3	Dakar 48/3000/50	3000	90.0	4.8
4	SMA Sunny Island 3324	3300	94.5	22
5	Trace SW3048	3300	95.0	16.0
6	Xantrex SW2548	2500	95.0	<20

As it can be seen in Table IV, the implemented prototype presents the best peak efficiency (96.0%). In comparison with an inverter of 95.0% (at the same output power), the apparently small difference of 1% corresponds to loss reduction of 20%. For example, processing 1000 W at 95% efficiency would result in 50 W of losses, whereas at 96%, only 40 W would be lost (this reduction of 10 W equals to 20% of 50 W). At the end, this saving can imply a lower working temperature and, consequently, a longer lifetime.

With regard to the no-load consumption, the proposed inverter presents a reasonable value if it is considered that it only competes with inverters 2 and 5. In fact, inverter 3 cannot be used as a reference because of its poor efficiency characteristic, and inverters 6 and 4 present higher no-load consumption allied to the worst peak efficiency.

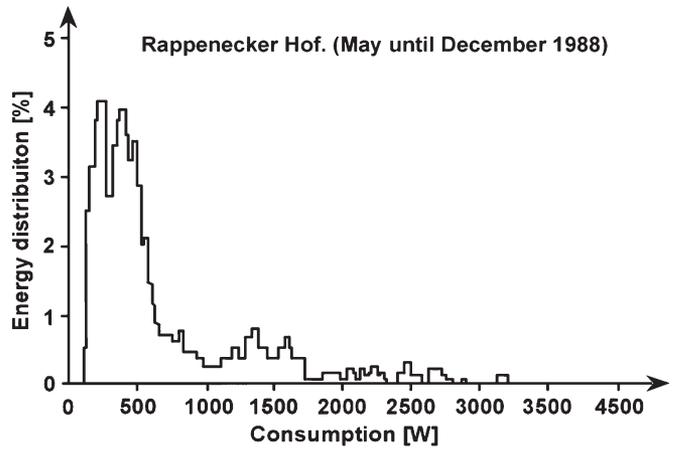


Fig. 13. Load profile of a typical stand-alone system (Rappenecker Hof [35]).

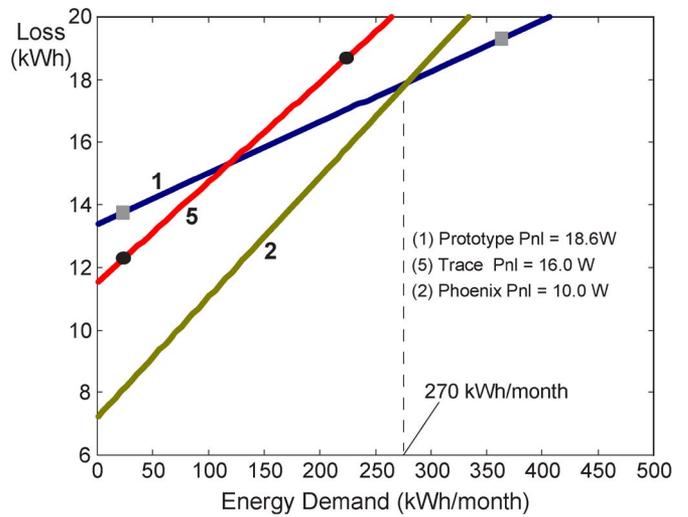


Fig. 14. Monthly energy loss versus processed energy.

Fig. 13 shows a typical load profile of a stand-alone SARES, indicating that most of the energy is processed at a fraction of its rated power. This is an important aspect to be considered in the inverter design, showing that it should be optimized to present high efficiency at low-power operation.

Considering now the aforementioned factors (efficiency characteristic, no-load consumption, and load profile), it is possible to plot the energy loss versus the total energy processed over a period of one month, as shown in Fig. 14. As it can be seen, inverter 2 presents a lower loss for any energy demand of up to approximately 270 kWh/month (average: 375 W), and above this value, the proposed inverter is more efficient. In comparison with inverter 5, the proposed inverter presents better efficiency for any energy demand above approximately 120 kWh/month.

### V. CONCLUSION

Most SARES store energy in battery banks to overcome the intermittence problem commonly found in RE sources, and a special battery inverter is necessary to guarantee continuous operation. Even more, it was concluded that either dc or ac bus-based systems demand on at least one reliable and robust

battery inverter, which should be capable of directly attending all consumer ac loads. It is proposed that this current demand on high-performance battery inverters can be reached by using multilevel topologies, and it is shown that the most suitable topologies are the multiple transformer and the multiwinding transformer. The implemented prototype was based on the multiwinding-transformer topology, and it has proved itself to be robust, presenting peak efficiency of 96.0%. The proposed inverter can be considered a top-efficiency inverter for the power range of about 3 kVA.

#### ACKNOWLEDGMENT

The authors would like to thank ISET, DeMoTec, UFC/GPEC, CAPES, and CNPq for supporting this research.

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