Microprocessor-Based DC Motor Drive with Spillover Field Weakening

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Abstract—**This paper describes a microprocessor-based speed control scheme for a separately excited dc motor fed from a dc source, which incorporates both armature-voltage control and spillover field weakening to provide smooth and precise control from standstill to speeds well above the base value. Armature-current limitation during transient operation is achieved using an interventionist system external to the microprocessor controller, thereby simplifying considerably the overall system design. Experimental results obtained from a prototype 5-kW drive are presented in the paper, to illustrate the excellent dynamic behavior of the scheme.**

I. Introduction

THE widespread use of microprocessor-based control systems arises from the many significant advantages they have over their analog counterparts. These include hardware simplicity, ease of changing the control strategy and parameters, immunity from temperature variations, and aging and cost of the system. There are few industrial situations in which microprocessor controllers are not now employed, and a number of publications, e.g. [1]–[4], have described their application to the speed control of dc motors.

The familiar expression for the speed ω of a separately excited dc motor

$$\omega = \frac{\text{applied armature voltage} - \text{armature volt drop}}{\text{constant} \times \text{flux/pole}}$$

shows that the speed may be adjusted by either armature voltage or field flux control. The former gives control up to base speed (corresponding to rated voltage) and has provided the basis for many schemes [1]–[3], whereas the latter gives control above base speed. A 20-kW drive using both forms of control has been described [4], although no indication is given of how the transition between the two forms of control was achieved at the base speed boundary.

It is obviously important that a drive incorporating both armature and field control should employ only a single-input demand throughout the speed range, and this is best achieved using spillover field weakening. When the demand speed is below or equal to the base speed, the speed error is eliminated by controlling the armature voltage while keeping the field flux constant at its maximum value. When either the speed demand is greater than the base speed, or the armature voltage for steady-state conditions exceeds an arbitrarily chosen figure of about 90% of the rated value, the armature voltage is held at this figure while the speed is controlled by varying the field flux. The 10% reserve of armature voltage is used to ensure a fast response following any sudden load change as the electrical time constant of the armature circuit is much smaller than that of the field circuit. Clearly, the changeover from armature to field control needs to be achieved automatically within the speed controller.

This paper describes the application of a microprocessor in a wide-range speed control system for a separately excited 5-kW dc motor using spillover field weakening and fed from a dc power source. Armature–voltage control is obtained using a four-quadrant high-frequency dc chopper and field control by a single-quadrant dc chopper. To limit the armature current during transient operation, a current-control loop operating in an interventionist mode is included in the control system.

II. Power Circuit

Fig. 1 shows schematically the power supply circuits used with the separately excited motor. The switching devices S1 to S4 in the H-bridge chopper are power MOSFET's, whereas D1 to D4 are epitaxial fast-recovery diodes. The unipolar switching strategy [5] was adopted for the chopper, as this produces less output voltage and current ripple than does the alternative bipolar switching strategy and is consequently more efficient. For forward operation of the chopper, S3 is open and S2 is closed, whereas S1 and S4 switch alternately with a fixed-frequency PWM signal. For reverse operation the state of the switches is S1 open and S4 closed, whereas S3 and S2 switch alternately with the PWM signal. The quadrant of operation is determined by the conducting devices, such that in the first quadrant S1 and S2 or S2 and D4 conduct; in the second quadrant D1 and D2 or S4 and D2 conduct; in the third quadrant S3 and S4 or S4 and D2 conduct and in the fourth quadrant D3 and D4 or S2 and D4 conduct. Fig. 2(a) shows idealized armature voltage and current waveforms (V_a and I_a, respectively) and the device-conduction pattern for first-quadrant operation (V_a positive, $I_a > 0$), and Fig. 2(b) presents corresponding information for second-quadrant operation (V_a positive, $I_a < 0$). In both cases, the mean armature voltage $\bar{V}_a$ is related to the direct supply voltage V_{dc} by

$$\bar{V}_a = \frac{t_{on a}}{T_a} V_{dc}$$

where $t_{on a}$ is the device "on" time defined in Fig. 2(a) and

Manuscript received February 15, 1991; revised August 26, 1991.

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IEEE Log Number 9103884.

0278-0046/91$01.00

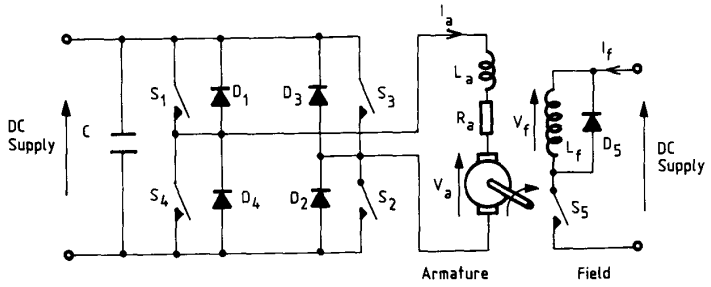

Fig. 1. Schematic diagram of power supply circuits.

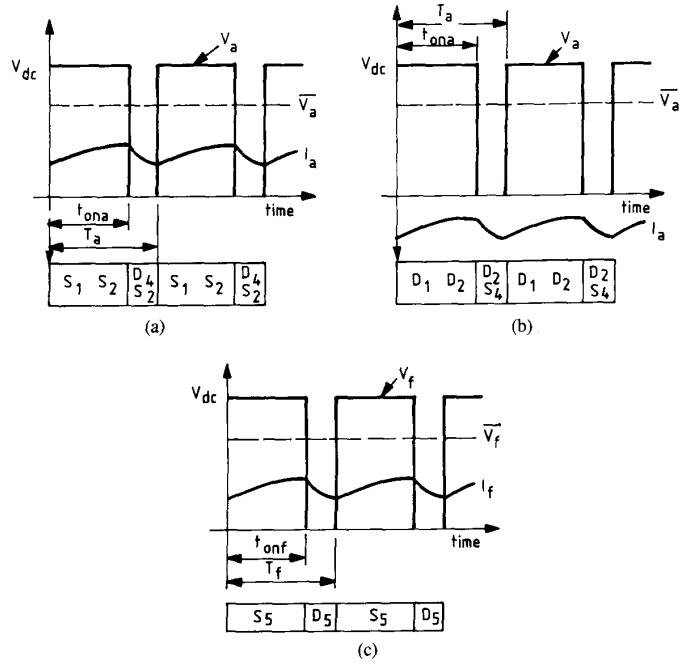

Fig. 2. Idealized voltage and current waveforms. (a) Armature circuit; first-quadrant operation. (b) Armature circuit; second-quadrant operation. (c) Field circuit.

(b) and T_a is the period of the armature chopper PWM signal. The PWM switching frequency was obtained by dividing down the microprocessor clock frequency. A value of 31 kHz was found to be suitable, being above the audible range and sufficiently high for the armature current ripple to be small but not so high that unacceptable switching losses are produced.

The switching device S5 for the field chopper is again a power MOSFET and D5 again an epitaxial fast-recovery diode. From the idealized voltage and current waveforms given in Fig. 2(c) the mean field voltage $\overline{V}_f$ follows as

$$\overline{V}_f = \frac{t_{\text{on}f}}{T_f} V_{\text{dc}}$$

where $t_{\text{on}f}$ is the "on" time of switch S5 and T_f the period of the field chopper PWM signal. The field chopper PWM switching frequency for the prototype system was also derived from the microprocessor clock frequency and, because the field circuit time constant is several times that of the armature circuit, a reduced frequency of 10 kHz was used.

The function of the microprocessor is to control the "on" times ($t_{\text{on}a}$ and $t_{\text{on}f}$) of the two choppers in order to vary the armature and field voltages in accordance with the speed control requirements.

III. Armature Current Control

Current control is usually achieved using either a regulating or an interventionist system [6]. In a regulating system, an inner current loop is continually active and is surrounded by an outer speed loop, with the speed error signal setting the reference current for the current loop. With an interventionist system the current loop is not normally operative but overrides the speed loop whenever the controlled current exceeds a limit set by the current controller.

An important feature of the interventionist system is that it provides a rapid speed response as there are no inherent delays associated with the filtering of the current feedback signal that is necessary in a regulating system. The interventionist system was therefore chosen to provide armature-current control.

As shown in Fig. 3(a), the current limiter comprises both sensing and comparator circuits. Current sensing is achieved using a precision Hall-effect current transformer, which provides electrical isolation between the high-voltage power circuit and the low-voltage control circuit. In four-quadrant operation, the current may be either positive or negative and the precision rectifier of Fig. 3(a) produces a unidirectional signal proportional to the armature current. The output of the rectifier is scaled by the amplifier SCA before being compared with the dc voltage level, which sets the current limit. The output of the comparator is applied to a deadband comparator with upper and lower limits of V_H and V_L, respectively. When the armature current I_a attempts to exceed the maximum value I_{max} shown in Fig. 3(b), and set by the upper deadband limit V_H, the output of the comparator goes low, inhibiting the drive signals to the armature chopper switches. The current therefore decays, and when it attempts to drop below the minimum value I_{min}, set by the lower deadband limit V_L, the comparator output goes high, enabling the drive signals to the armature chopper. During periods of rapid acceleration or deceleration, the armature current cycles between I_{max} and I_{min} and, if these limits are sufficiently close, the armature current waveform appears to be flat topped, as is evident in the practical results presented in Section VI.

Care must clearly be taken in the design of an interventionist system to ensure that the current limit I_{max} of Fig. 3(b) is below the level that could lead to a commutation failure of the dc machine [6].

IV. Microprocessor Hardware

A layout of the controller hardware required to provide both armature and field control is shown in Fig. 4. To ensure that the resolution was sufficiently high, a 16-b Intel 8086 microprocessor was used with the inputs to and outputs from the microprocessor being interfaced with peripheral equipment using 8255A programmable peripheral interfaces.

The microprocessor input ports receive both demand-speed and speed-feedback signals. The demand speed is set by three hexabinary switches, which are interfaced to the input ports by a 12-b latch. The speed feedback is obtained from a 1000-pulse/revolution incremental encoder, with the encoder output pulses being counted by a 12-b counter over a sampling period of 15 ms. At the end of this time the count value, which represents the motor speed, is supplied to the processor and the counter is reset for the next sampling period.

The processor outputs two 8-bit numbers, which control the turn-on times of the armature and field choppers. The PWM waveform controlling the armature chopper switches is generated using the duty cycle generator circuit of Fig. 5, with the 8-b counter performing a full count in 32 μs, which is the chopper period. The output of the counter is applied to input B of the comparator and the processor output is applied to input A. During the time when the value of the processor output is less than the counter output, the comparator output B > A is low. Because the processor output sets the duty interval t_{on_a}, this output is inverted as shown in Fig. 5. The four drive signals to the armature chopper for forward operation with a 50% duty cycle are shown in Fig. 6. Signals for switches S2 and S3 are set by the direction of the speed demand (forward operation) and those for switches S1 and S4 by the output of the comparator and its complement. A built-in delay of 1.2 μs is incorporated between the turn-off time of devices S1 and the turn-on time of the complementary device S4, and vice versa, to prevent shoot-through of the dc supply.

V. Controller Design

A. Simulation

A digital controller may be designed either directly in the z plane using a discrete model of the system or in the conventional analogue manner using well-established s plane techniques with a final conversion to the z plane. The latter method was followed in the present situation due to the existence of many well-proven analogue design techniques.

The experimental drive was investigated in closed-loop using an interactive simulation and analysis IBM software package called SIMBOL, which can simulate linear, nonlinear, and digital control systems. The system to be modeled, shown in Fig. 7, was described interactively on the computer screen using standard block diagram transfer functions, and the dynamic characteristics were investigated using both frequency-response and time-domain simulations. Initially, the controller was assumed to contain an integral term only, with a transfer function $C_i(s) = k_i/s$. It was evident after several simulations using different integrator constants that, although the steady-state error was eliminated, a satisfactory time response could not be achieved with this arrangement. For a fast well-damped response with negligible overshoot, the closed-loop response plotted on a Nichols chart should be around the 0-dB closed-loop contour. For a value $k_i = 5$, a maximum phase lag of 30° at a system frequency of 30 rad/s was required to meet this condition and this was achieved using a lag term of the form

$$C_{LG}(s) = \frac{0.019s + 1}{0.058s + 1}.$$

The theoretical time response with this controller was satisfactory, but when the scheme was implemented in the actual system the speed response exhibited a large overshoot due to the action of the current limiter, and this could not be eliminated even by reducing the value of k_i. This feature demonstrated the need for the controller to provide damping and the lag network was accordingly replaced by a lead network, which approximates to a proportional-plus-derivative controller. Successive simulations, taking as an initial step the time constants of the lag controller above, gave a lead network with the transfer function

$$C_{LD}(s) = \frac{0.29s + 1}{0.09s + 1}$$

cascaded with an integral controller of the form $C_I(s) = 2.6/s$, to give an overall controller transfer function

$$C(s) = \frac{2.6(0.29s + 1)}{s(0.09s + 1)}. \quad (1)$$

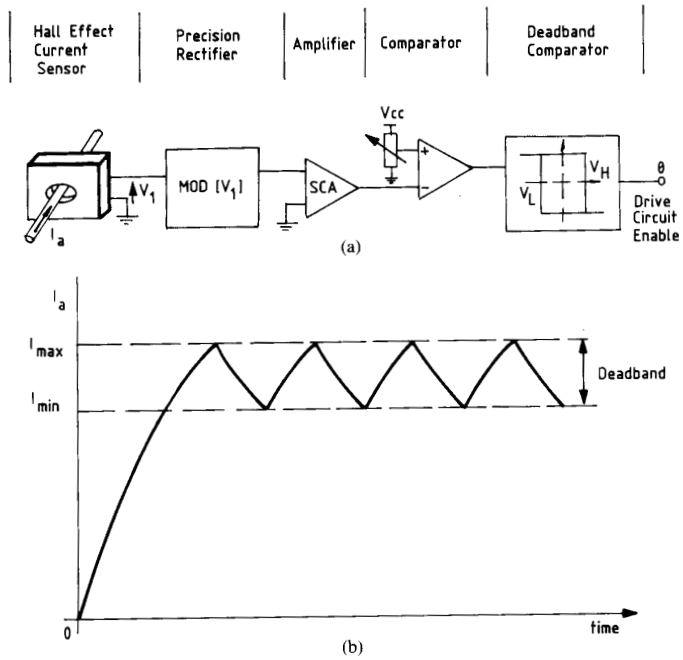

Fig. 3. Current limit circuit. (a) Block diagram. (b) Armature current waveform.

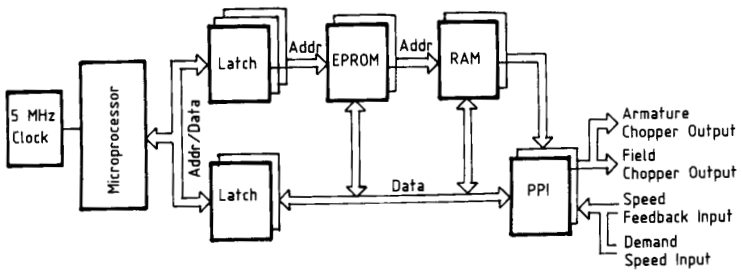

Fig. 4. Microprocessor hardware layout.

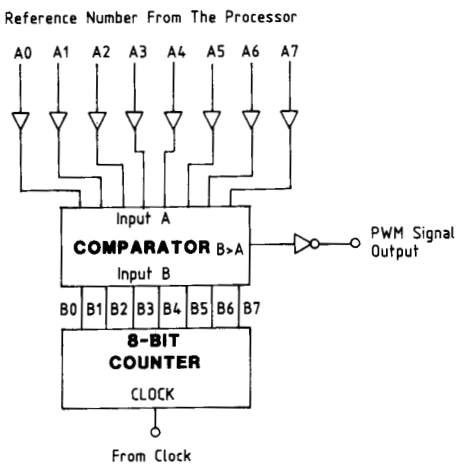

Fig. 5. Duty cycle generator.

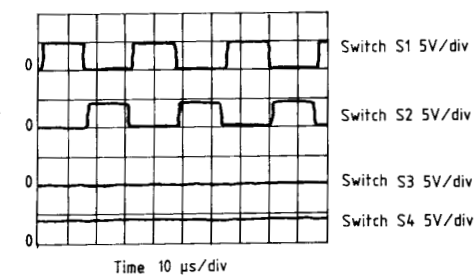

Fig. 6. Armature chopper drive signals; 50% duty cycle.

B. Emulation

The process of transforming the analog s plane representation for the controller into the digital z plane representation is termed "emulation" [7]. Defining the relationship between s and z as

$$s = \frac{2(z-1)}{T_s(z+1)}$$

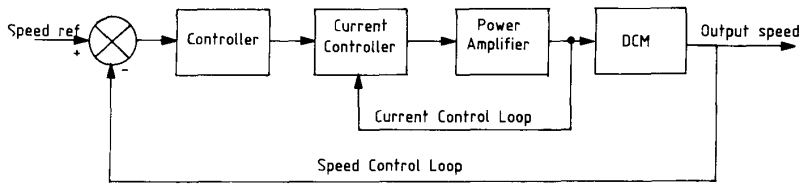

Fig. 7. Closed-loop system to be modeled.

where T_s is the sampling time, leads from (1) to a controller transfer function in the z plane as

$$C(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \tag{2}$$

where $a_0 = 0.0788$, $a_1 = 0.0031$, $a_2 = 0.0716$, $b_1 = 1.8007$, and $b_2 = 0.8007$. The performance of the integrator is greatly effected by the accuracy with which the above coefficients are defined, and it is frequently better to define the transfer function in terms of the δ operator as this is much less sensitive to coefficient inaccuracy [8]. The δ operator is defined as

$$z = \delta + 1$$

which, when substituted in (2), gives

$$C(\delta) = \frac{C_0 + C_1\delta^{-1} + C_2\delta^{-2}}{1 + r_1\delta^{-1} + r_2\delta^{-2}} \tag{3}$$

where

$$C_0 = a_0, \quad C_1 = 2a_0 + a_1 \quad C_2 = a_0 + a_1 + a_2$$
$$r_1 = 2 + b_1 \quad \text{and} \quad r_2 = 1 + b_1 + b_2.$$

Equation (3) may be represented diagrammatically by Fig. 8(a), which is restructured in Fig. 8(b) to obtain the set of difference equations describing the controller

$$\begin{aligned} D_2(nT_s) &= D_1((n-1)T_s) + D_2((n-1)T_s) \\ D_1(nT_s) &= D_1((n-1)T_s) + 0.1993X_a((n-1)T_s) \\ X_a(nT_s) &= X_i(nT_s) - D_1(nT_s) \\ X_0(nT_s) &= 0.0788X_a(nT_s) + 0.8070D_1(nT_s) \\ &\quad + 0.052D_2(nT_s) \end{aligned} \tag{4}$$

These equations were used in the microprocessor software to control the armature chopper duty cycle according to the speed error, as explained in the next section.

C. Controller Software

The controller software was written in the assembly language ASM 86 for Intel microprocessors. A simplified flowchart of the program is shown in Fig. 9 and this is cycled through once every sampling period. Initially, the field duty cycle is set to a maximum to give maximum flux. The direction of rotation is read, and this defines the state of the armature chopper switches. The demand speed n_d is then read and compared with the base speed n_b. According to the result of this comparison, and whether the error between n_d

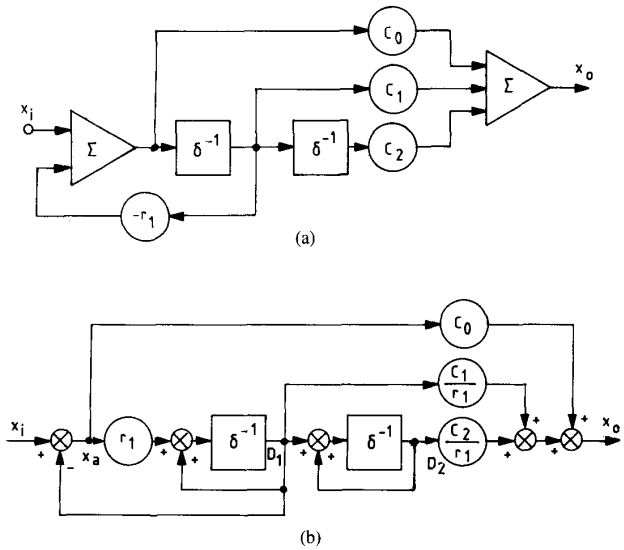

Fig. 8. Filter structure. (a) With δ operator. (b) Modified arrangement.

and the actual speed n is within a certain error band, four controller operations are possible.

Control 1 – $n_d > n_b$ and n Approaching n_d: If the armature chopper is duty cycle $t_{ona} > 90\%$ of its maximum value, the field chopper duty cycle is reduced by 2%. This allows a reduction in t_{ona}, until the 10% margin is available. The steady-state error is eventually eliminated by armature-voltage control using the difference equations (4).

Control 2 – $n_d > n_b$ and n Not Close to n_d: The armature chopper duty cycle is maintained at its maximum value. The field duty cycle is held at its maximum until n approaches n_b, after which the field duty cycle is reduced by 2% every time control 2 is implemented. When the speed error is acceptable, control 1 trims t_{ona} and eliminates the steady-state error.

Control 3 – $n_d < n_b$ and n Approaching n_d: Armature-voltage control is used to eliminate the steady-state error. If $t_{ona} > 90\%$ of its maximum value, the field chopper duty cycle is trimmed as explained for control 1.

Control 4 – $n_d < n_b$ and n Not Close to n_d: Both the armature and field chopper duty cycles are held at their maximum values until n approaches n_d, at which point the steady-state error is eliminated by armature-voltage control.

Cycling through the program, the controller modifies the armature and field chopper duty cycles until the steady-state speed error is eliminated. At times of rapid acceleration and deceleration, when the motor demands a large armature

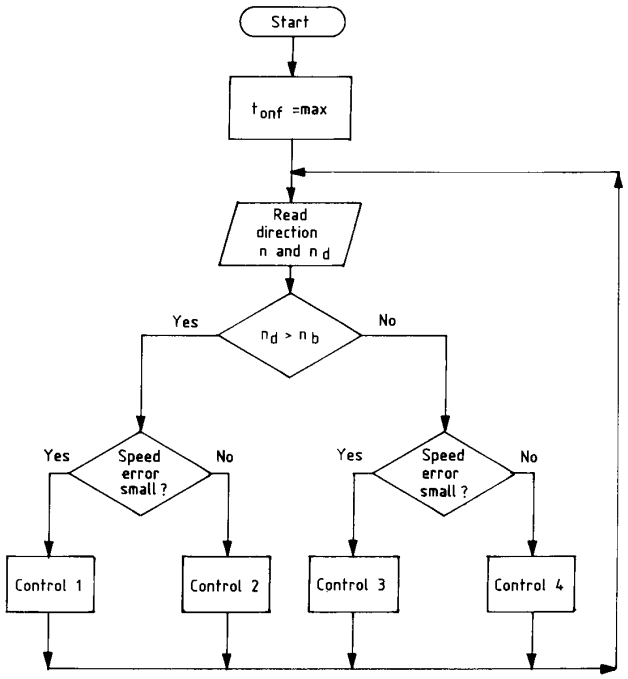

Fig. 9. Flowchart of controller software.

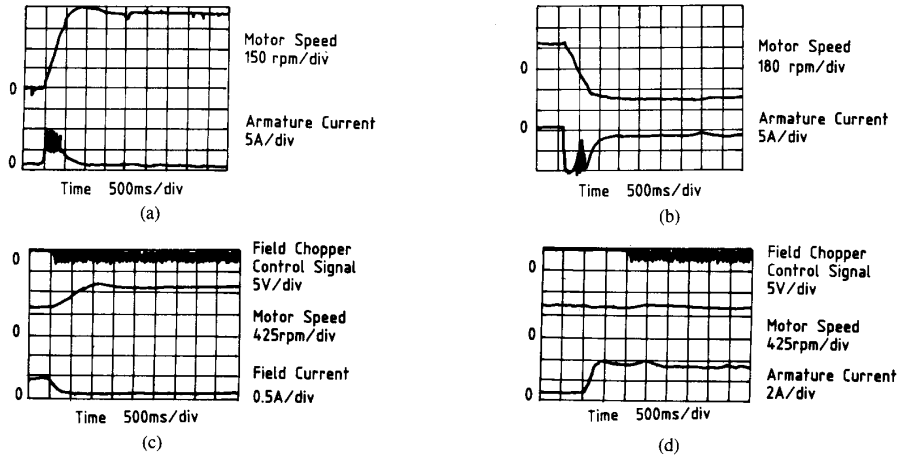

Fig. 10. Transient response: experimental results. (a) Sudden change in demand speed, below base speed. (b) Sudden reversal of demand speed. (c) Sudden change in demand speed, above base speed. (d) Sudden change in load at base speed.

current, the current controller inhibits the signals to the armature chopper switches, as explained in Section III.

VI. Experimental Results

The experimental results presented in Fig. 10 illustrate the dynamic performance of the speed-control system when used with the experimental 5-kW 230-V motor. Fig. 10(a) shows the speed response following a sudden change in demand speed from 150–750 r/min (the base value), with the armature current limitation provided by the current loop being evident during the period of rapid acceleration. The machine slightly overshoots the demand speed before settling to within $\pm 5\%$ of this speed in about 1 s. Fig. 10(b) shows the response to a sudden reversal of demand speed. In this case the armature current remains clamped at its negative maximum during the period of deceleration and subsequent acceleration in the reverse direction. Fig. 10(c) shows the response to a step change from base speed to maximum speed. Initially, the field chopper duty cycle is 100% but, as the motor speeds up, the duty cycle reduces with a consequent reduction in the field current and motor flux. It is evident that field control produces a slower response than does armature control, due to the relatively long field-time constant. As mentioned in Section I, there are situations when the field

flux is reduced even though the motor is running at or below base speed. Fig. 10(d) shows the motor running on no-load at base speed, when full-load torque is suddenly applied. The speed drops and the armature duty cycle increases in an attempt to raise the motor speed. However, the armature duty cycle reaches its maximum value before the motor speed attains its original value and armature control is unable to provide a further speed increase. On detecting that the armature voltage is maximum and the presence of a constant speed error, the processor reduces the field duty cycle, enabling the motor speed to increase. The armature duty cycle is reduced as the motor speeds up, leaving some armature voltage for any sudden acceleration requirements.

VII. Conclusions

This paper has described a microprocessor-controlled four-quadrant dc drive that combines armature-voltage control with spillover field weakening. The microprocessor implementation is flexible as the entire control techniques can be changed simply by loading new software, as was demonstrated when the lag-integral control was replaced by the lead-integral control.

In the experimental setup, the maximum error at maximum speed (1100 r/min) was 4 r/min or 0.39%. This error arises because the armature voltage is not infinitely variable but depends on the digital 8-b number that represents the armature chopper duty cycle. The armature voltage therefore changes in steps of $\frac{1}{256}$ of the dc bridge voltage.

The current limiter provides accurate and reliable current limiting in all four quadrants. The method has the advantage of relying on the interventionist principle, so that the design of the speed control loop is not compromised by that of the current loop and there is no need to filter the current signal.

A novel structure for the recursive filter was used, which is much less sensitive to coefficient inaccuracy than other structural forms and required minimal computational effort, which is of primary importance in such real-time digital control applications.

Acknowledgment

Mr. Antunes gratefully acknowledges the financial support provided by the Brazilian government throughout his postgraduate studies at Loughborough University of Technology.

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