Interleaved-Boost Converter With High Voltage Gain

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***Abstract*—This paper presents an interleaved-boost converter, magnetically coupled to a voltage-doubler circuit, which provides a voltage gain far higher than that of the conventional boost topology. Besides, this converter has low-voltage stress across the switches, natural-voltage balancing between output capacitors, low-input current ripple, and magnetic components operating with the double of switching frequency. These features make this converter suitable to applications where a large voltage step-up is demanded, such as grid-connected systems based on battery storage, renewable energies, and uninterruptible power system applications. Operation principle, main equations, theoretical waveforms, control strategy, dynamic modeling, and digital implementation are provided. Experimental results are also presented validating the proposed topology.**

***Index Terms*—DC–DC converter, large voltage step-up, low-voltage stress, renewable energies, uninterruptible power system (UPS).**

I. Introduction

THE USE of batteries and photovoltaic panels as the primary source in autonomous systems has become more and more common in order to provide clean electric energy. Thus, to transfer the energy from conventional batteries (12 or 24 V_{dc}) to conventional 110/220 V_{rms} ac systems, it is necessary to step the battery voltage up using a dc–dc converter.

Though conventional boost converter can theoretically be used for this purpose, obtaining such high voltage gain implies that it would operate with duty cycles greater than 0.9, which is not feasible due to the great variations in the output voltage caused by small variations in the duty cycle, leading the boost converter to instability. Also, in practice, the parasitic elements due to the losses associated with the converter components do not allow a voltage step-up larger than six times [1].

To obtain the desired voltage, boost converters can be connected in cascade, or a high frequency isolation dc–dc converter with high transformer turns-ratio can be used instead, even though efficiency is reduced due to a greater number of stages. Another alternative is to use an inverter with low-frequency transformer on the input stage. However, this solution compromises the structure volume, weight, and efficiency.

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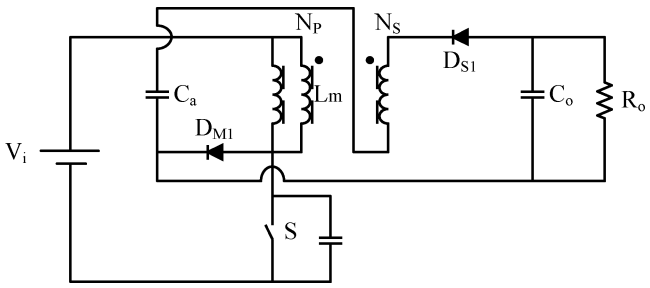

Fig. 1. Topology proposed in [4].

To overcome this drawback, some solutions using step-up converters capable of operating with large voltage step-up were proposed in [2]–[25]. In [2], the author proposes an arrangement with numerous magnetic elements connected through semiconductor devices in order to obtain large conversion ratios. However, the proposed structure presents low efficiency due to the large number of processing stages and high control complexity, as it uses many switches.

In [3] and [4], Zhao *et al.* proposed the use of a clamp-mode coupled-inductor buck-boost converter, as presented in Fig. 1, which provides high voltage gain combined with low-voltage stress across the switches, minimizing conduction losses. However, the main disadvantages observed on these converters were their pulsating input current and high current stress through the clamping capacitors. In [5], Huber and Jovanovic propose the use of cascade-boost converters, but the circuit becomes complex and costly.

In [6] and [7], the use of an interleaved-boost converter associated with an isolated transformer was introduced, using the high frequency ac link. Despite the good performance, the topology uses three magnetic cores, which prejudice the weight, the volume, and the efficiency of the structure.

An interleaved-boost converter with high static gain employing multiplier capacitors connected in series was proposed in [8]. This converter, shown in Fig. 2, presents low-input current ripple and low-voltage stress across the switches. However, high current flows through the series capacitors at high power levels. In [9]–[13], converters with high static gain based on the boost-flyback topology are introduced. These converters present low-voltage stress across the switches, but the input current is pulsed, as it needs an *LC* input filter.

The step-up switching-mode converter with high voltage gain using a switched-capacitor circuit was proposed in [14]–[19]. This idea is only adequate for the development of low-power converters, since high peak currents appear through the semiconductors, due to the charging dynamics on the switched capacitors. Besides, it results in high-voltage stress across the switches, and thus, many capacitors are necessary.

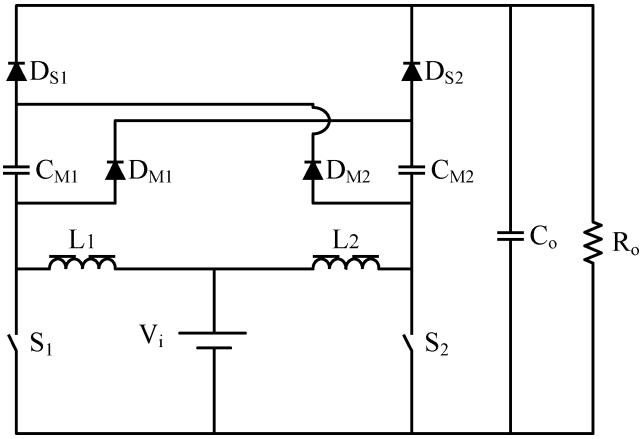

Fig. 2. Topology proposed in [8].

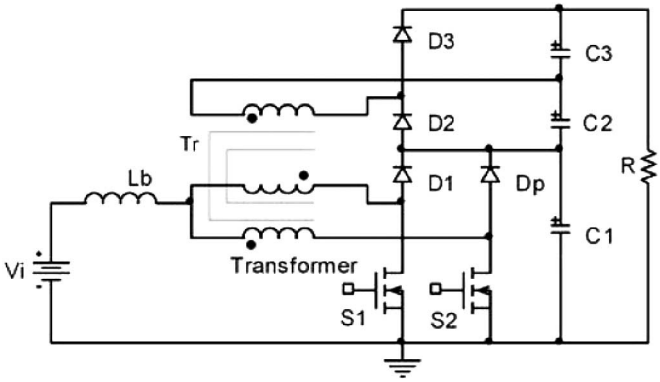

Fig. 3. Topology proposed in [29].

A quadratic-boost converter associated to a nondissipative soft-switching cell is presented in [23]. This converter can operate with large voltage scale and no isolation between the power and the control stages are required. However, the series association of the switch with the diode increases the conduction losses.

Recently, other converters have been proposed, as proposed in [24]–[31]. In [24]–[27], a family of interleaved high step-up boost converters with winding-cross-coupled inductors is presented, where a modified-coupled inductor with three windings and its third winding inserted into another phase is proposed, achieving good performance. In [28] and [29], the three-state switching cell is presented as shown in Fig. 3. Nonpulsated with low-ripple input current and low-voltage stress across the switches are the main benefits of the proposed topology, however, the duty cycle is limited, as it must be higher than 0.5, and the inductors are rather large. In [30], a voltage-doubler rectifier is employed as the output stage of an interleaved-boost converter with coupled inductors, but low efficiency is achieved. In [31], the authors introduce the concept of coupled inductors combined with switched capacitors. However, this idea is only adequate to low power applications.

This paper introduces an interleaved-boost converter with high output voltage. The proposed converter increases, by far, the conventional boost gain using magnetic coupling, as discussed in the following.

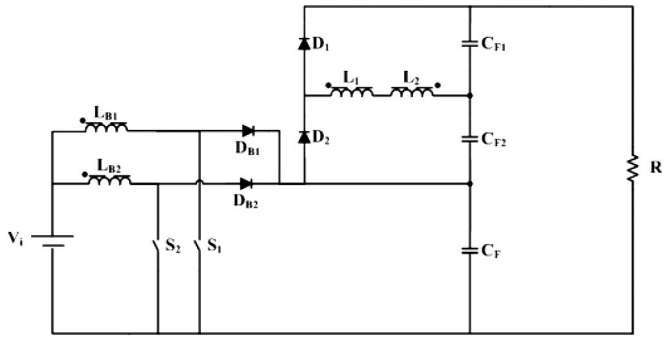

Fig. 4. Proposed high-voltage-gain boost converter.

II. High-Voltage-Gain Boost Converter

This section presents the operation principle, equations, and main theoretical waveforms of the proposed converter operating in continuous conduction mode. In order to obtain such high gain, a voltage-doubler circuit is magnetically coupled to the conventional–interleaved boost (L_{B1} with L_1, and L_{B2} with L_2), as can be seen in Fig. 4. Also, the number of semiconductor devices is the same as in the traditional interleaved-boost arrangement, though two coupled inductors L_1 and L_2 are added, resulting in higher output voltage. The interleaved-boost switching cycle is composed of four stages, as detailed in the following.

A. Operation Principle and Main Theoretical Waveforms

For the theoretical analysis, it will be considered that input and output voltages are ripple free and all devices are ideal. Also, prior to the first stage, it will be considered that both switches were turned on, and L_{B1} and L_{B2} charged. It also must be noticed that the duty cycle shall never be lesser than 50%, as there would be no energy transfer from the transformer's primary side to the secondary one. It is also important to notice that the switching cycles of both switches S_1 and S_2 should be the same, as this condition avoids misbalances between the currents through L_{B1} and L_{B2}, and the voltages across the output capacitors.

1) First Stage [t_0–t_1]: At t_0, S_1 is turned off and S_2 is maintained turned on, as shown in Fig. 5. Thus, the energy is now transferred to the capacitor C_{F2} due to the magnetic coupling between L_{B1} and L_1, and L_{B2} and L_2. It must be noticed that the voltage across switch S_1 is clamped by the voltage across capacitor C_F, which is only a third of the output voltage considering a unitary transformer turns-ratio. Also, the average currents through D_{B1} and through the magnetically coupled cell are equal to the half of the output current and to the output current, respectively. Equations (1) and (2) present the Kirchhoff voltage law through the circuit loops containing L_{B1} and L_{B2}, respectively, while relation (3) shows the voltage relations on the coupled cell. At t_1, S_1 is turned on finishing

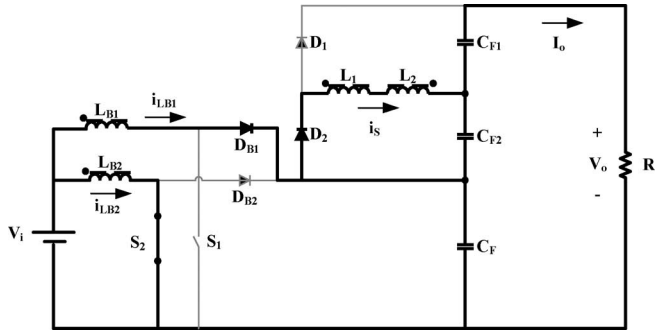

Fig. 5. First stage.

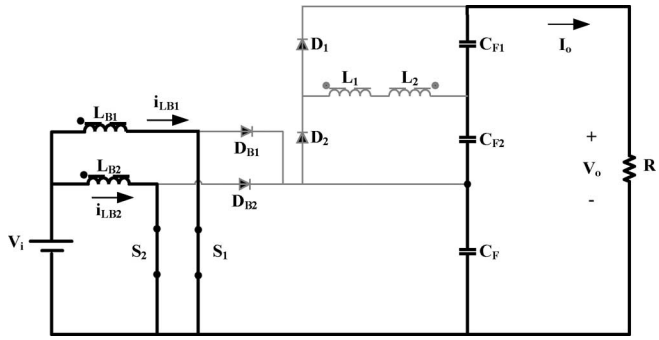

Fig. 6. Second and fourth stages.

this stage

$$V_{C_F} + L_{B1}\frac{di_{L_{B1}}}{dt} + M\frac{di_s}{dt} - V_i = 0 \tag{1}$$

$$L_{B2}\frac{di_{L_{B2}}}{dt} - M\frac{di_s}{dt} - V_i = 0 \tag{2}$$

$$V_{C_{F2}} = \left(-nL_{B2}\frac{di_s}{dt} + M\frac{di_{L_{B2}}}{dt}\right) - \left(nL_{B1}\frac{di_s}{dt} + M\frac{di_{L_{B1}}}{dt}\right) \tag{3}$$

where M is the mutual inductance and k is the magnetic coupling coefficient, given by (4) and (5), respectively,

$$M = nkL_{B1} \tag{4}$$

$$k = \frac{V_{L_1}}{nV_{L_{B_1}}}. \tag{5}$$

2) Second Stage [t_1–t_2]: At instant t_1, switch S_1 is turned on while S_2 remains turned on. The second stage is illustrated in Fig. 6, where the energy is being stored in L_{B1} and L_{B2}, though it keeps flowing to the secondary, due to the transformer characteristic assumed by the inductors during this stage. Besides, L_{B1} starts storing energy again. This period ends at the instant t_2, when S_2 is turned off. The equations that represent this stage are

$$L_{B1}\frac{di_{L_{B1}}}{dt} - V_i = 0 \tag{6}$$

$$L_{B2}\frac{di_{L_{B2}}}{dt} - V_i = 0. \tag{7}$$

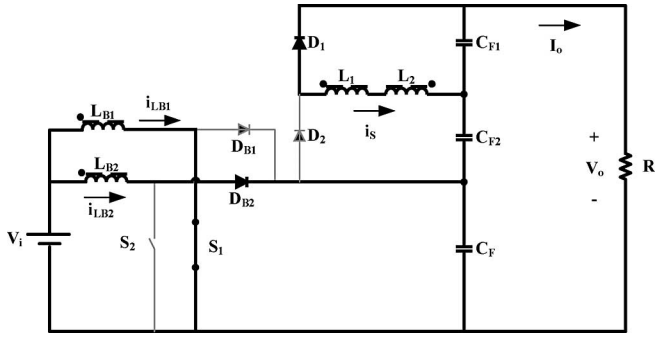

Fig. 7. Third stage.

3) Third Stage [t_2–t_3]: This stage begins when switch S_2 is turned off, as shown in Fig. 7. The previously stored energy in L_{B2} is transferred to the capacitor C_{F1} due to the magnetic coupling between L_{B2} and L_2. Similar to the first stage, the voltage across S_2 is clamped by the voltage across capacitor C_F. The average current through D_{B2} is equal to the one in D_{B1}, specified on the first stage, and the same occurs with the average current through the magnetically coupled cell. The equations that define this stage are similar to the relations presented in the first one. This stage ends when S_2 turns on again.

4) Fourth Stage [t_3–t_4]: This stage is similar to the second one: when the two switches are turned on, the energy is stored on both inductors, though it keeps flowing to the secondary, as shown in Fig. 6. This stage ends when S_1 is turned off, backing again to the first stage.

From Fig. 8, the main theoretical waveforms can be observed, which illustrate the details of the operation principle stages explained earlier.

B. Static Gain

The output voltage at any given moment can be expressed as the sum of the voltages across each output capacitors C_F, C_{F1}, and C_{F2}, as presented in (8)

$$V_o = V_{C_F} + V_{C_{F1}} + V_{C_{F2}}. \tag{8}$$

Relation (9) can be obtained observing that the voltage across the inductors L_{B1} and L_{B2} must be null during a switching-cycle period. Thus, the voltage across the capacitor V_{C_F} can be expressed by (10)

$$DV_i = (1-D)(V_{C_F} - V_i) \tag{9}$$

$$V_{C_F} = V_i\frac{1}{1-D}. \tag{10}$$

In order to express the voltage across C_{F2}, and thus across C_{F1}, as they are equivalent due to the similarity between them, the stages that present energy transfer between the coupled inductors must be observed. Considering $L_{B1} = L_{B2}$, relation (11) can be obtained from (1)–(3). Also, the current flowing through the coupling cell can be expressed as in (12). Thus, by integrating (11) and equaling to (12), it is possible to

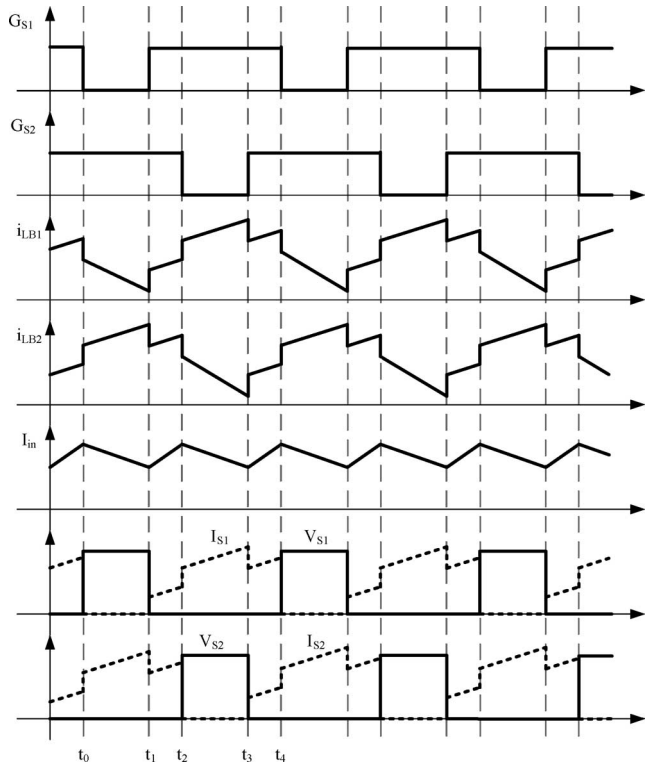

Fig. 8. Main theoretical waveforms.

determine $V_{C_{F2}}$

$$\frac{di_s}{dt} = \frac{(1-D)V_{C_{F2}}L_{B1} - MV_i}{2(1-D)\left(M^2 - nL_{L_{B1}}^2\right)} \tag{11}$$

$$i_s = C\frac{dV_{C_{F2}}}{dt} + \frac{V_{C_{F2}}}{R} \tag{12}$$

$$V_{C_{F2}} = \frac{MRT_sV_i}{2\left(M^2 - nL_{B1}^2\right) + (1-D)LRT_s}. \tag{13}$$

For normal project conditions, the first term of the denominator is far lesser than the second one. Thus, simplifying relation (13) and substituting M for the relation presented in (4), $V_{C_{F2}}$ and $V_{C_{F1}}$ can be expressed as (14)

$$V_{C_{F1}} = V_{C_{F2}} = V_i\frac{nk}{(1-D)}. \tag{14}$$

Substituting (10) and (14) in (8), the expression of the static gain G can be obtained as presented in (15). Also, Fig. 9 illustrates the relation between the static gain and the duty cycle ($G \times D$), for different values of transformer turns-ratio (n), and magnetic coupling coefficient (k). It must be noticed from this figure that, even though a unitary transformer turns-ratio is adopted, the static voltage gain is far higher than the one obtained using a conventional-boost converter, even with the duty cycle near 50%

$$G = \frac{V_o}{V_i} = \frac{(2nk)+1}{1-D}. \tag{15}$$

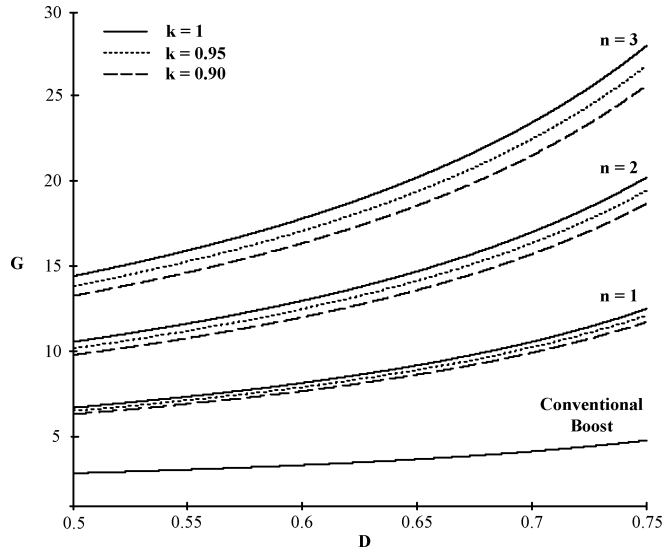

Fig. 9. Relation $G \times D$ for different values of n and k.

C. Design Approach

From (1) and (2), it is possible to determine the behavior of the currents through L_{B1} and L_{B2}. For simplification, it will be assumed the following condition (16):

$$I_{L_{B1\,\mathrm{med}}} = I_{L_{B1\,\mathrm{ef}}} = \frac{I_{\mathrm{in}}}{2}. \tag{16}$$

Equations (17) and (18) determine how to obtain the inductances on the primary and secondary sides

$$L_{B1} = L_{B2} = L_B = \frac{V_iD}{2\Delta I_{\mathrm{in}}f_s} \tag{17}$$

$$L_1 = L_2 = n^2L_B. \tag{18}$$

The maximum voltage stress across switches S_1 and S_2 is equal to the voltage across capacitor C_F, as expressed in (19). Average and rms currents through the switches are given by (20) and (21), respectively,

$$V_{S1\,\max} = V_{S2\,\max} = V_{C_{F\,\max}} = V_i\frac{1}{1-D_{\max}} \tag{19}$$

$$I_{S1\mathrm{med}} = I_{S2\mathrm{med}} = D\frac{I_{\mathrm{in}}}{2} \tag{20}$$

$$I_{S1\mathrm{ef}} = I_{S2\mathrm{ef}} = \sqrt{D}\frac{I_{\mathrm{in}}}{2}. \tag{21}$$

From aforementioned equations, it is possible to express the average and the rms currents on D_{B1} and D_{B2}, given by (22) and (23), respectively. The maximum reverse voltage across D_{B1} and D_{B2} is defined by (24)

$$I_{D_{B1\,\mathrm{med}}} = I_{D_{B2\,\mathrm{med}}} = (1-D)\frac{I_{\mathrm{in}}}{2} \tag{22}$$

$$I_{D_{B1\,\mathrm{ef}}} = I_{D_{B2\,\mathrm{ef}}} = \left(1-\sqrt{D}\right)\frac{I_{\mathrm{in}}}{2} \tag{23}$$

$$V_{D_{B1\,\max}} = V_{D_{B2\,\max}} = -V_{C_F} = -V_i\frac{1}{1-D_{\max}}. \tag{24}$$

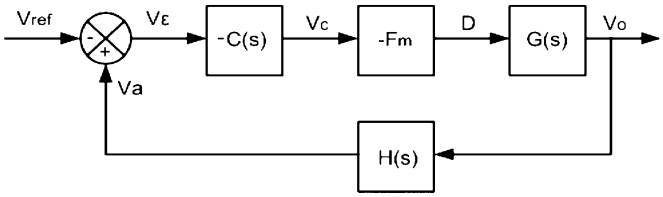

Fig. 10. System block diagram.

In order to maintain the voltages on the output capacitors equilibrated, it is necessary that the average current through diodes D_1 and D_2 be equal to the output current, as expressed in (25). Equations (26) and (27) define the rms current and the maximum reverse voltage on these diodes, respectively,

$$I_{D_{1\,\mathrm{med}}} = I_{D_{2\,\mathrm{med}}} = I_o \tag{25}$$

$$I_{D_{1\,\mathrm{ef}}} = I_{D_{2\,\mathrm{ef}}} = \sqrt{1-D}\frac{I_{\mathrm{in}}}{2} \tag{26}$$

$$V_{D_{1\,\mathrm{max}}} = V_{D_{2\,\mathrm{max}}} = -V_{C_{F1}} = -V_i\frac{n}{1-D_{\mathrm{max}}}. \tag{27}$$

Finally, (28) presents the voltage ripple across the three output capacitors. This relation can be obtained analyzing the second stage, where the load current flows through the output capacitors

$$\Delta v_{C_F} = \Delta v_{C_{F1}} = \Delta v_{C_{F2}} = \frac{I_o}{C_F}\left[\frac{T_s}{2} - (1-D)\,T_s\right]. \tag{28}$$

III. Control Strategy and Dynamic Modeling

A. Voltage-Control Loop

This section presents the control strategy used in order to guarantee the stability of the converter's output voltage, considering load variations. The block diagram of the voltage loop control is illustrated in Fig. 10. This technique consists in sampling the output voltage and comparing it to a reference, which generates an error voltage. This error serves as a parameter to the compensator, providing the control voltage, which, after the modulation, provides pulsewidth modulation pulses for driving switches, with adjusted duty cycle for stabling output voltage on the desired level. The obtained signals from the control circuit are presented in Fig. 11.

From Fig. 11

$$t_{\mathrm{ON}} = D2T_s \tag{29}$$

$$t'_{\mathrm{ON}} = (1-D)\,2T_s. \tag{30}$$

According to the triangle similarity, observing the carrier and the reference voltage signals in Fig. 11

$$\frac{\Delta v_c}{v_c} = \frac{T_s}{t'_{\mathrm{ON}}} \tag{31}$$

$$t'_{\mathrm{ON}} = T_s\frac{1}{\Delta v_c}v_c. \tag{32}$$

From (30) and (32)

$$D = 1 - \frac{1}{2\Delta v_c}v_c. \tag{33}$$

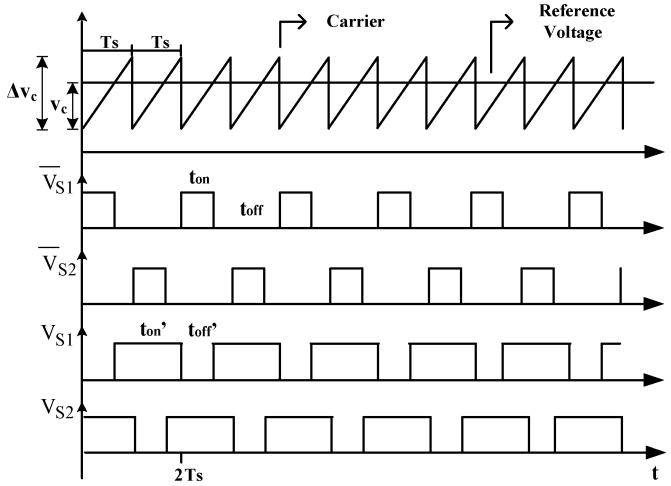

Fig. 11. Signals from the control circuit.

Derivation of (33) shows the behavior of duty cycle variation implied from voltage variation, presented in (34), which leads to the modulator gain, given by (35)

$$\frac{\partial D}{\partial v_c} = -\frac{1}{2\Delta v_c} \tag{34}$$

$$F_m = -\frac{1}{2\Delta v_c}. \tag{35}$$

In order to avoid the phase introduction of -180°, it is considered that the modulator negative signal is cancelled by the signal inversion of the compensator. Thus

$$F_m = \frac{1}{2\Delta v_c}. \tag{36}$$

B. Compensator Design

The compensator project aims to guarantee the system stability. The first step is to determine the transfer function that relates output voltage with duty cycle. For the proposed converter, the same function used for the basic boost converter has been adopted [35], [36]

$$G(s) = \frac{(V_{\mathrm{in}}/(1-D)^2)(1-(s/(R_0(1-D)^2))L_{B1})}{s^2(L_{B1}C_{\mathrm{Bosst\_eq}}/(1-D)^2) + s(L_{B1}/(R_0(1-D)^2)) + 1}. \tag{37}$$

The equivalent capacitance of the proposed topology $C_{F\mathrm{eq}}$ is the value seen by the source, and it is calculated as follows:

$$\frac{1}{C_{F\mathrm{eq}}} = \frac{1}{C_{F1}} + \frac{1}{C_{F2}} + \frac{1}{C_F}. \tag{38}$$

Following the energy-conservation principle, it is possible to convert $C_{F\mathrm{eq}}$ into $C_{\mathrm{BOOST\_eq}}$, which is the capacitance of the equivalent conventional boost

$$\frac{1}{2}C_{\mathrm{Boost\_eq}}V^2_{\mathrm{Boost\_eq}} = \frac{1}{2}C_{F\mathrm{eq}}V^2_{\mathrm{Proposed\_Boost}} \tag{39}$$

$$C_{\mathrm{Boost\_eq}} = 2.04\,\mathrm{mF}. \tag{40}$$

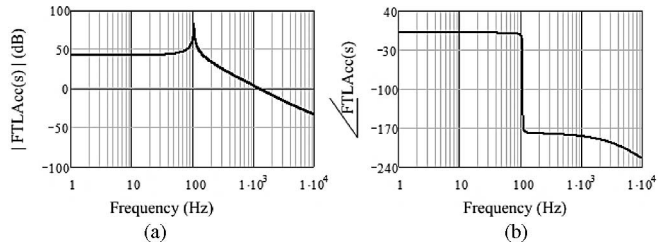

Fig. 12. Predicted system transfer function Bode diagram. (a) Gain. (b) Phase.

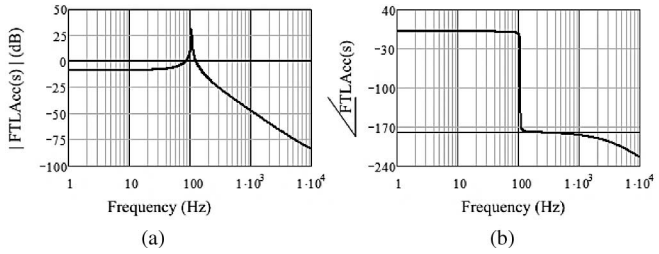

Fig. 13. Predicted noncompensated system Bode diagram. (a) Gain. (b) Phase.

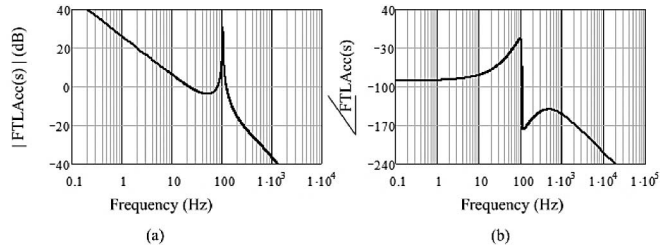

Fig. 14. Predicted compensated system Bode diagram. (a) Gain. (b) Phase.

Substituting the projected values in (37)

$$G(s) = \frac{-0.002123s + 132.3}{1.909 \times 10^{-5}s^2 + 1.604 \times 10^{-5}s + 1}. \quad (41)$$

Fig. 12 presents the Bode diagram of the system-transfer function (41). It is important to notice that the converter presents a zero on the right semiplane, which can direct the system to instability.

The second step is to calculate the open-loop-transfer function $\mathrm{FTLA_{sc}}(s)$

$$\mathrm{FTLA_{sc}}(s) = G(s)F_m H(s). \quad (42)$$

Fig. 13 illustrates the Bode diagram of $\mathrm{FTLA_{sc}}(s)$. It can be noticed the small gain in lower frequencies, an inclination higher than –20 dB/dec on crossing frequency, and phase margin near zero. Thus, the noncompensated system tends to instability.

In order to control the voltage loop, it was chosen a PID compensator. The Bode diagram of the open-loop-transfer function with the compensator is shown in Fig. 14, where it can be observed that the function has a phase margin of 111° and a gain near to –20 dB/dec, which has proven to be experimentally stable.

TABLE I
CONVERTER SPECIFICATIONS

Input Voltage	16 - 28 Vdc
Output Voltage	180 Vdc
Nominal Power	500 W
Switching Frequency	50kHz
Transformer turns ratio (n)	1
Inductances of L_{B1}, L_{B2}, L_1, and L_2	220µH
Capacitances of C_F, C_{F1}, and C_{F2}	680µF

TABLE II
EMPLOYED COMPONENT PARAMETERS

Capacitors	EPCOS B43840
Capacitors ESR	0.120Ω
Inductors Average ESR	0.011Ω
Switches S_1 and S_2	IRFP4710
S_1 and S_2 Turn-on Resistance	0.014Ω
Boost Diodes D_{B1} and D_{B2}	HFA25PB60
D_{B1} and D_{B2} Voltage Drop	1.3V
Magnetic Couple Cell Diodes D_1 and D_2	MUR460
D_1 and D_2 Voltage Drop	1.25V

C. Digital-Control Design

In order to convert the compensator-transfer function from the s-plane to the z-plane, making this function discrete, it used the Tustin method with a sample time of 200 μs, chosen because it is the period that the digital controller takes to read the A/D channel and execute the following instructions for each loop control. The system blocks of the gain relative to the A/D and the D/A converters were also added. By making some approximations, the equation to be introduced on the micro controller is given by

$$U(k) = 2U(k-1) - 1U(k-2) + \frac{6}{10}e(k) - \frac{12}{10}e(k-1) + \frac{6}{10}e(k-2). \quad (43)$$

IV. EXPERIMENTAL RESULTS

In order to verify the validity of the proposed topology, a prototype has been built to demonstrate the effectiveness of the converter. Its specifications and the employed component parameters are presented in Tables I and II, respectively. The choice of large output capacitors was made based on predicting the use of an inverter connected to the converter output, which would require large capacitors in order to attenuate the low-frequency ripple.

Fig. 15 presents the input and the output voltages when the input is only 16 $\mathrm{V_{dc}}$, and the output is still regulated on 180 $\mathrm{V_{dc}}$, proving the effectiveness of the proposed converter, where a voltage gain of about 11 times is obtained.

Fig. 16 shows the waveforms from the voltage and the current through S_1, where it can be observed that the low voltage stress through the main switches is only a third of the output voltage. Fig. 17 presents the balancing between the currents flowing through the inductors L_{B1} and L_{B2}.

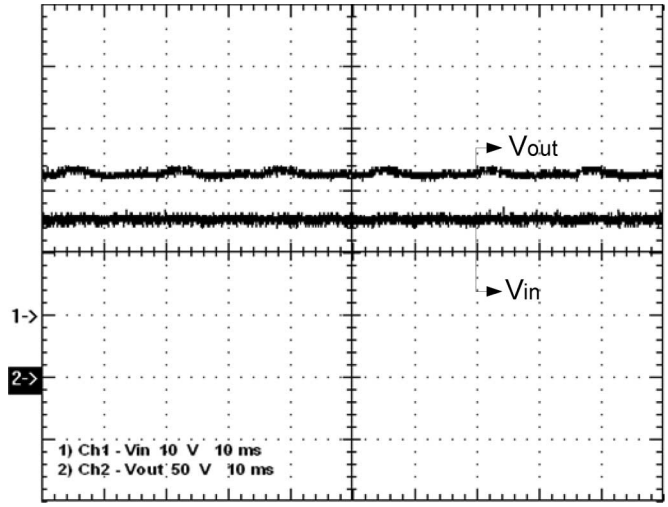

Fig. 15. Input (10 V/div) and output (50 V/div) voltages.

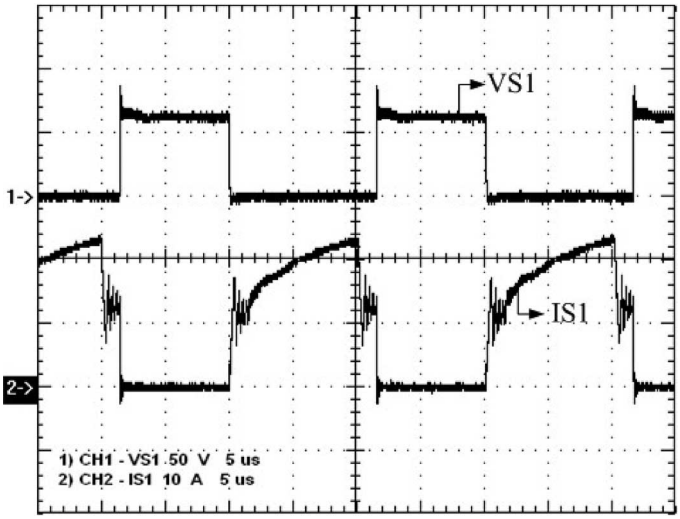

Fig. 16. Voltage (50 V/div) and current (10 A/div) through switch S_1.

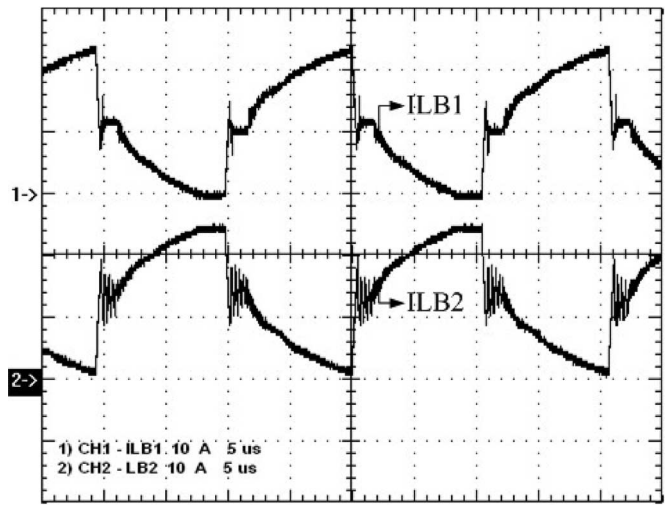

Fig. 17. Currents through L_{B1} and L_{B2} (10 A/div).

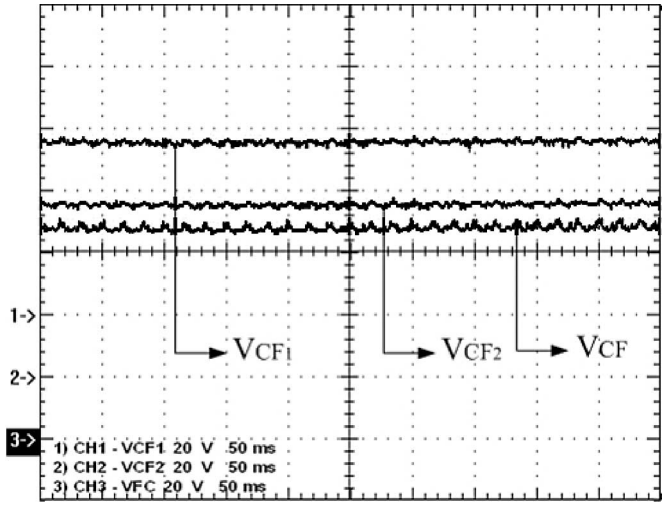

Fig. 18. Voltages across the output capacitors (20 V/div).

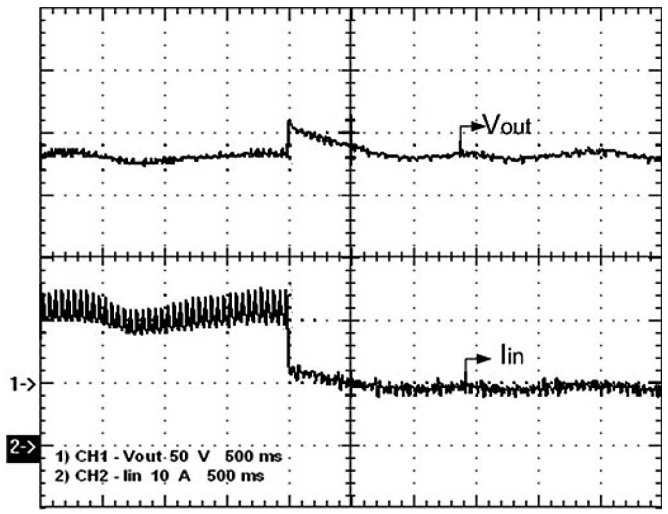

Fig. 19. Output voltage and current under load step from 500 to 250 W.

Fig. 18 shows the voltage balancing between the output capacitors. It must be noticed that the small difference on V_{C_F} compared to $V_{C_{F1}}$ and $V_{C_{F2}}$, according to (9) and (13), is due to the dependence of V_{C_F} only on the duty cycle, while $V_{C_{F1}}$ and $V_{C_{F2}}$ are dependent on the duty cycle, the transformer turns relation, and the leakage inductance.

Figs. 19 and 20 present the dynamic behavior of the proposed converter. In Fig. 19, a load step from 500 to 250 W was applied, causing an overshoot of 30 V, corresponding to a variation of 16.67%. In Fig. 20, the load step was from 250 to 500 W, causing an overshoot of 25 V, corresponding to a variation of 13.88%. However, instead of this initial variation noticed on both cases, the output voltage was able to return to its previous condition, as expected. It also must be observed that the slow-time response is limited by the speed of the available micro controller used on the project.

Fig. 21 presents the converter-efficiency curve. It must be noticed that, at the nominal power, the converter has achieved an

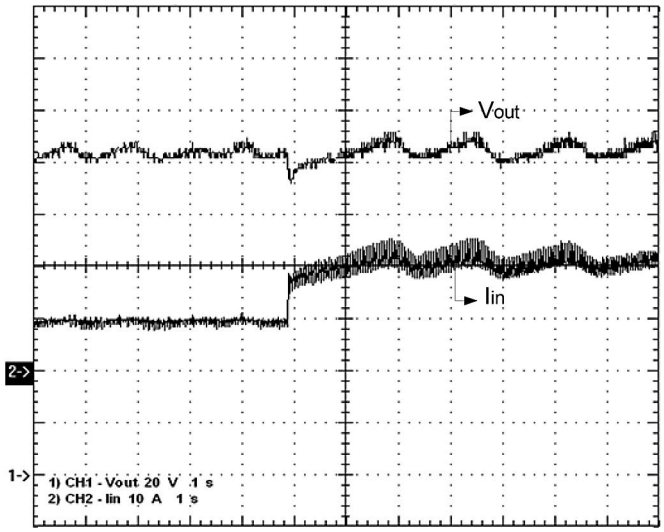

Fig. 20. Output voltage and current under load step from 250 to 500 W.

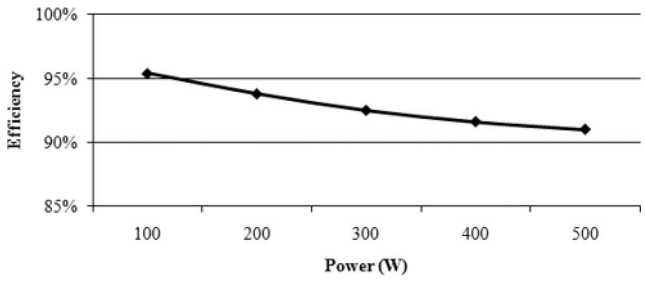

Fig. 21. Efficiency curve of the converter.

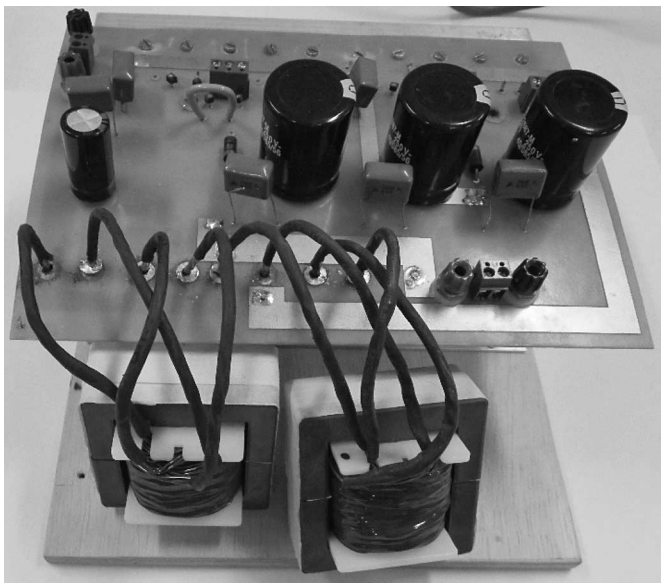

Fig. 22. Power stage prototype picture.

efficiency of 91%, while the best measured efficiency was 95.4% at 100 W. It also must be considered that no soft-switching cells were used on the main switches, which would probably make the efficiency even higher. Finally, Fig. 22 presents the power stage prototype picture.

V. Conclusion

An interleaved-boost converter with high voltage gain was presented, and its equations, operation principle, and main theoretical waveforms were all detailed. The topology presents, as a main feature, a large voltage step-up with reduced voltage stress across the main switches, important when employed in grid-connected systems based on battery storage, like renewable energy systems and uninterruptible power system applications.

Other characteristics of the converter are: voltage balancing between output capacitors, low input-current ripple, high switching frequency, which reduce the structure volume and weight, simple switching control, as just a simple voltage-loop control based on the conventional boost was implemented, and the possibility to make the voltage gain even higher by increasing the transformer turns-ratio.

The main drawbacks related to this topology are the duty cycle limitation, as it must be higher than 50%, and the need of a soft start and initial charge of output capacitors, common in topologies deriving from conventional boost converters.

Finally, the proposed converter had shown its effectiveness proved through experimental results, as the project of the digitally implemented voltage-loop control. Still, some improvements can be obtained by achieving better performance on the converter efficiency.

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