DC–DC Nonisolated Boost Converter Based on the Three-State Switching Cell and Voltage Multiplier Cells

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***Abstract*—This work introduces a dc–dc boost converter based on the three-state switching cell and voltage multiplier cells. A brief literature review is presented to demonstrate some advantages and inherent limitations of several topologies that are typically used in voltage step-up applications. The behavior of the converter is analyzed through an extensive theoretical analysis, while its performance is investigated by experimental results obtained from a 1-kW laboratory prototype, as relevant issues are discussed. The converter can be applied to uninterruptible power supplies and is also adequate to operate as a high gain boost stage cascaded with inverters in renewable energy systems. Furthermore, it can be applied to systems that demand dc voltage step up such as electrical fork-lift, renewable energy conversion systems, and many other applications.**

***Index Terms*—Boost converters, dc–dc converters, high voltage gain, voltage multiplier cells (VMCs).**

I. Introduction

DEPENDING on the application nature, several types of static power converters are demanded for the adequate conversion and conditioning of the energy provided by primary sources such as photovoltaic arrays, wind turbines, and fuel cells. Moreover, considering that the overall cost of renewable energy systems is high, the use of high efficiency power electronic converters is a must [1].

Literature presents numerous examples for applications where dc–dc step-up stages are necessary, e.g., photovoltaic systems [2], uninterruptible power supplies (UPSs) [3], fuel cell powered systems [4], and fork-lift vehicles [5], although many other ones can be easily found. Typical solutions include the use of low-frequency or high-frequency power transformers to adjust the voltage gain properly. In addition, galvanic isolation may be necessary due to safety reasons [6]. Unfortunately, this practice may bring increased size, weight, and volume if compared with nonisolated approaches such as the boost converter.

Manuscript received December 2, 2011; revised February 17, 2012, May 18, 2012, and July 11, 2012; accepted August 11, 2012. Date of publication August 16, 2012; date of current version May 16, 2013.

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Digital Object Identifier 10.1109/TIE.2012.2213555

The conventional boost converter can be advantageous for step-up applications that do not demand very high voltage gains mainly due to the resulting low conduction loss and design simplicity [7]. Theoretically, the boost converter static gain tends to be infinite when duty cycle also tends to unity. However, in practical terms, such gain is limited by the I^2R losses in the boost inductor and semiconductor devices due to their intrinsic resistances, also leading to the necessity of accurate and high-cost drive circuitry for the active switch [8].

Due to the importance of the conventional boost converter in obtaining distinct and improved topologies for voltage step-up applications, some techniques have been developed and modified with the aim of improving the characteristics of the original structure. Basically, two strategies are adopted for this purpose: voltage step-up with and without using extreme values of duty cycle. Some arrangements existent in literature will be discussed as follows.

An early work concerned with nonisolated converters with large conversion ratios was proposed in [9], where multiple stages are connected in parallel to obtain high voltage step-up converters. However, the use of multiple controlled switches, diodes, and inductors may lead to high component count, making the proposed approach not adequate to achieve very large ratios that are typically obtained with the use of transformers.

Cascading one or more boost converters may be considered to obtain high voltage gain. Even though more than one power processing stage exists, the operation in continuous conduction mode (CCM) may still lead to high efficiency [10]. The main drawbacks in this case are increased complexity and the need for two sets including active switches, magnetics, and controllers [11]. Due to high power levels and high output voltage, the latter cascaded boost stage has severe reverse losses, with consequent low efficiency and high electromagnetic interference (EMI) levels. Typical examples of such topologies are the single-switch quadratic boost converter and the two-switch three-level boost converter [12].

Converters with magnetically coupled inductance such as flyback or SEPIC can easily achieve high voltage gain using switches with reduced on-resistance, even though efficiency is compromised by the losses due to the leakage inductance [13]. An active clamping circuit is able to regenerate the leakage energy, at the cost of increased complexity and some loss in the auxiliary circuit [14].

A hybrid boost-flyback converter is introduced in [15]. The efficiency of the conventional flyback structure is typically low due to the parasitic inductance. A possible solution lies in connecting the output of the boost converter to that of the flyback topology, with consequent increase of voltage gain due to the existent coupling between the arrangements. In this case, the boost convert behaves as an active clamping circuit when the main switch of the flyback stage is turned off.

A boost converter using switched capacitors is proposed in [16], where high voltage gain can be obtained, but it is restricted to low power applications. In this case, the dc output voltage can be increased as desired by adding a given number of capacitors. Low duty cycle is used, alleviating the problem of the boost diode reverse recovery. However, the high component count with distinct voltage ratings is an inherent drawback.

As the power rating increases, it is often required to associate converters in series or in parallel. For high-power high-current applications with voltage step-up characteristic, interleaving of two boost converters is usually employed to improve performance and reduce size of magnetics. Furthermore, the currents through the switches become just fractions of the input current. Interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, as the size of the energy storage inductors and differential-mode EMI filter in interleaved implementations can be reduced [17]. The converter studied in [18] uses two boost topologies coupled through an autotransformer with unity turns ratio and opposite polarity so that the current is equally shared between the switches. Moreover, voltage doubler characteristic is achieved. Even though the current stress through the switches is reduced, their voltage stress is less than or equal to half the total output voltage. Isolated drive circuitry must also be employed in this case.

Other topologies using the interleaving technique are investigated in [19] and [20]. Voltage multiplier cells (VMCs) are adopted to provide high voltage gain and reduced voltage stress across the semiconductor elements. Interleaving also allows the operation of the multiplier stages with reduction of the current stress through the devices. In addition, size of input inductors and capacitors is drastically reduced. The voltage stress across the main switches is limited to half of the output voltage for a single multiplier stage. However, high component count is necessary, with the addition of a snubber circuit due to sum of the reverse recovery currents through the multiplier diodes and consequent increase of conduction losses.

The topology studied in [21] uses a voltage doubler rectifier as the output stage of an interleaved boost converter with coupled inductors. High voltage gain can be obtained, although efficiency is compromised by the use of a RCD snubber.

In the last few years, some converters based on the three-state switching cell (3SSC) have been proposed as a prominent solution for high current applications and will be discussed as follows. The 3SSC can be obtained by the association of two two-state pulse width modulation (PWM) cells (2SSC) interconnected to a center tap autotransformer, from which a family of dc–dc converters can be derived. This concept was first introduced in [22], as the so-called cell type B is obtained.

The topology investigated in [23] uses VMCs associated with the 3SSC to achieve high voltage gains in high-power high-current applications. This circuit is based on 3SSC boost converter, whose claimed advantages are: the input current is continuous with low ripple; the input inductor is designed for twice the switching frequency, with consequent weight and volume reduction; the voltage stress across the switches is lower than half of the output voltage, and naturally clamped by one output filter capacitor. As possible drawbacks, a small snubber is necessary for each switch, and one additional winding per cell is required for the autotransformer, associated with high component count and increased size and weight of the transformer [23].

The converter proposed in [24] presents high voltage gain and is a particular case of the previous approach [23], while the input current is continuous with reduced ripple. This topology is limited to one VMC coupled to one transformer secondary winding. The input inductor is also designed for twice the switching frequency, implying reduction of weight and size. The voltage stress across the switches is less than half of the output voltage due to clamping performed by the output filter. It is also important to mention that, for a given duty cycle, the output voltage can be increased by adjusting the transformer turns ratio without affecting the voltage stress across the main switches. Metal oxide semiconductor field effect transistors (MOSFETs) with reduced on-resistance can be used to further minimize conduction losses. However, the converter cannot operate adequately when duty cycle is lower than 0.5 due to magnetic induction issues. The hard commutation of switches and high component count are also possible drawbacks.

An isolated converter, whose characteristics are similar to those of the push converter, is introduced in [25]. The use of the 3SSC is associated with the following advantages: utilization of only one primary winding that allows the addition of a dc current blocking capacitor in series connection, in order to avoid the transformer saturation problem; less copper and reduced magnetic cores are involved during the transformer assembly; and the moderate leakage inductance of the transformer allows the reduction of the commutation losses of the switches. The autotransformer of the 3SSC has small size, because it is designed for half of the output power and for a high magnetic flux density, since the current through the windings is almost continuous with low ripple [25].

Within this context, this paper proposes a topology for high-current voltage step-up applications based on the use of multiplier cells constituted by diodes and capacitors. The converter is able to operate in overlapping (when duty cycle D is higher than 0.5) and nonoverlapping (when duty cycle D is lower than 0.5) modes, analogous to other 3SSC-based structures [4], [7], [22]–[25]. However, the study carried out in this paper only considers the operation with $D > 0.5$. This is a significant improvement if compared with the structure presented in [24], where the operation with duty cycle lower than 0.5 leads to poor performance of the transformer in terms of the secondary induced voltage, as it is not possible to step up the output voltage to the desired value.

The analysis is focused on a structure with two cells, aiming to determine the stress regarding the elements that constitute the aforementioned configuration. Experimental results regarding the topology are also presented and discussed to validate the proposal.

II. Proposed Topology

The canonical switching cell is an approach that allows obtaining and classifying the classical dc–dc converters, from which some families of converters can be derived [26]. Buck, boost, and buck-boost converters, which are second-order systems, as well as Cúk, SEPIC, and Zeta, which are fourth other systems, have a single switching cell that is part of their respective power stages. Literature has also shown appreciable effort to improve the characteristics of the original structures, even though the novel resulting topologies are more complex approaches with higher component count.

The 2SSC is composed by three terminals, which are active, passive, and common. Its behavior is based on the complementary operation of two switches connected by the common terminal. In other words, one switch is turned on while the remaining one remains turned off, and vice-versa. Therefore, this arrangement can be called 2SSC.

With the aim of achieving higher power density, switching frequency is usually increased, with consequent reduction of size and volume of reactive elements. Switching losses are consequently increased, while the volume of heat sinks also is. This practice therefore compromises the very reduction of physical dimensions in static power converters.

The aforementioned losses must then be reduced, and soft switching circuits using the resonance phenomenon have been widely proposed as a possible solution. By using well known techniques such as zero voltage switching and zero current switching, the performance of converters can be improved. However, even though switching losses are mitigated or eliminated, conduction losses are still of major concern and may even increase depending on the adopted snubber.

With the aim to further reduce voltage and/or current stress, the association of semiconductor or even converters in series or in parallel has been thoroughly investigated. Other topologies can also be obtained, such as multilevel converters [27].

It is also possible to increase the efficiency by the use of the 3SSC, which is derived from the dc–dc push-pull converter [22]. It is formed by two controlled switches S_1 and S_2, two diodes D_1 and D_2, one autotransformer T, and one inductor L. Even though the resulting cell seems more complex with higher component count than the conventional 2SSC, its advantages over its counterpart have been clearly demonstrated in several works [4], [7], [22]–[25], that are: the use of the 3SSC may lead to the need of switches with reduced current rating, which is desirable in high-power high-current applications; the area for which converters operate in CCM is wider [22]; the ripple current through the inductor is reduced; reactive elements are designed for twice the switching frequency, causing the required critical inductance to be smaller, for instance; only 50% of the power is delivered to the load through the main switches due to the magnetic coupling between the transformer windings [22].

Typically, a high-frequency transformer is used in static power converters to achieve high voltage conversion ratio, either in step-up or step-down applications. This practice eliminates the need to operate with extreme duty cycle values, even though additional loss due and increased size and weight associated with the transformer are the resulting disadvantages. For instance, let us consider the circuit of the interleaved flyback-boost converter mentioned in [27]. Even though the static gain becomes $N \cdot [1/1 - D)]$, where N is the turns ratio and D is the duty cycle, and the current rating of the main switches is reduced by the use of interleaving cells, the proposed approach does not contribute to the very reduction of conduction losses. In structures, using the 3SSC, this is an intrinsic and remarkable advantage [22].

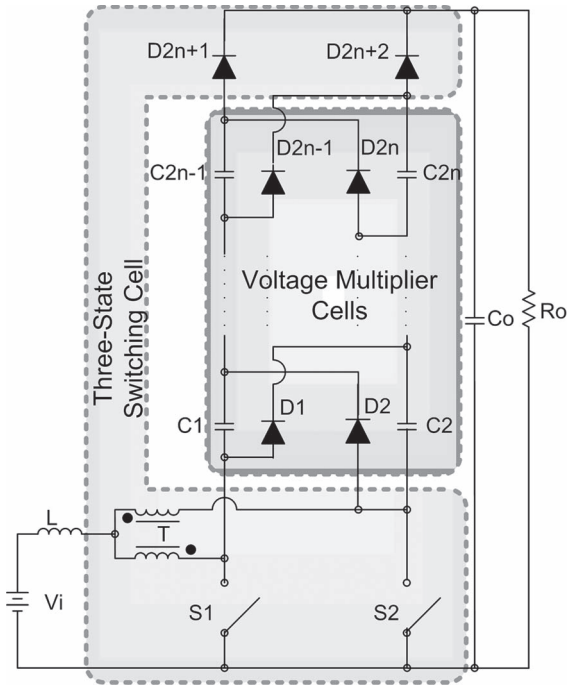


Fig. 1. Proposed boost converter based on the association of the three-state switching cell and voltage multiplier cells.

The use of voltage multiplier of cells is not new and has already been reported in literature. For instance, the work developed in [29] employs multiplier capacitors to achieve high voltage gain. A single switch is used, while high voltage and high current stress result. As it was mentioned before, the use of the 3SSC may be interesting for high-power high-current applications.

A generic version of the topology that uses the 3SSC and a given number of VMCs mc is shown in Fig. 1. The association of the VMC and the 3SSC results in the creation of a new switching cell, which can be used in the conception of novel buck, boost, buck-boost, Cúk, SEPIC, and Zeta topologies.

The analysis presented in this session considers the boost converter associated with two multiplier cells is and detailed as follows.

In order to better understand the operating principle of the structures, the following assumptions are made:

- the input voltage is lower than the output voltage;
- steady-state operation is considered;
- semiconductors and magnetics are ideal;
- switching frequency is constant;
- the turns ratio of the autotransformer is unity;
- the drive signal applied to the switches are 180° displaced.

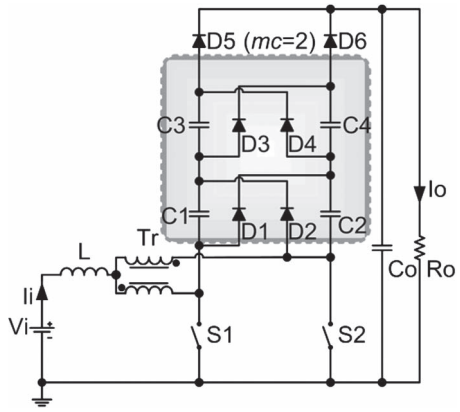


Fig. 2. Proposed converter using two voltage multiplier cells ($mc = 2$).

1) Operating Principle: The introduced concept can be extended to the use of two multiplier cells, as the resulting topology is presented in Fig. 2. The equivalent circuits that correspond to the converter operation and the relevant theoretical waveforms are presented in Figs. 3 and 4, respectively.

First stage $[t_0, t_1]$ [Fig. 3(a)]: Switches S_1 and S_2 are turned on, while all diodes are reverse biased. Energy is stored in inductor L, and there is no energy transfer to the load. The output capacitor C_o provides energy to the load. This stage finishes when switch S_1 is turned off.

Second stage $[t_1, t_2]$ [Fig. 3(b)]: While switch S_1 is turned off, switch S_2 remains turned on, and diode D_3 is forward biased. Energy is not transferred to the load in this stage yet, and the output capacitor C_o is still being discharged. However, energy is still provided to inductor L by the input voltage source V_i. Capacitor C_1 is discharged, and capacitors C_2 and C_4 are charged. This stage finishes when diode D_5 is forward biased.

Third stage $[t_2, t_3]$ [Fig. 3(c)]: Switches S_1 and S_2 remain turned off and turned on, respectively. Diodes D_3 remain forward biased, and diode D_5 also is, while the remaining diodes are reverse biased. Energy flows to the load through diode D_5, so that capacitor C_o is charged. The energy stored in inductor L is transferred to the output stage. Capacitors C_2 and C_4 are still charged, and capacitor C_3 starts being discharged. This stage finishes when diode D_3 is reverse biased.

Fourth stage $[t_3, t_4]$ [Fig. 3(d)]: Switch S_1 remains turned off, switch S_2 remains turned on, diodes D_1 and D_5 are forward biased, while diodes D_3 and the remaining ones are reverse biased. Energy is transferred to the output stage through diode D_5. Inductor L is discharged, capacitor C_2 is charged, and capacitors C_1 and C_3 are discharged. This stage finishes when diode D_1 is reverse biased.

Fifth stage $[t_4, t_5]$ [Fig. 3(e)]: This stage is identical to the first one.

Sixth stage $[t_5, t_6]$ [Fig. 3(f)]: This stage is analogous to the second one, even though switch S_1 is turned on and switch S_2 is turned off.

Seventh stage $[t_6, t_7]$ [Fig. 3(g)]: This stage is similar to the third one.

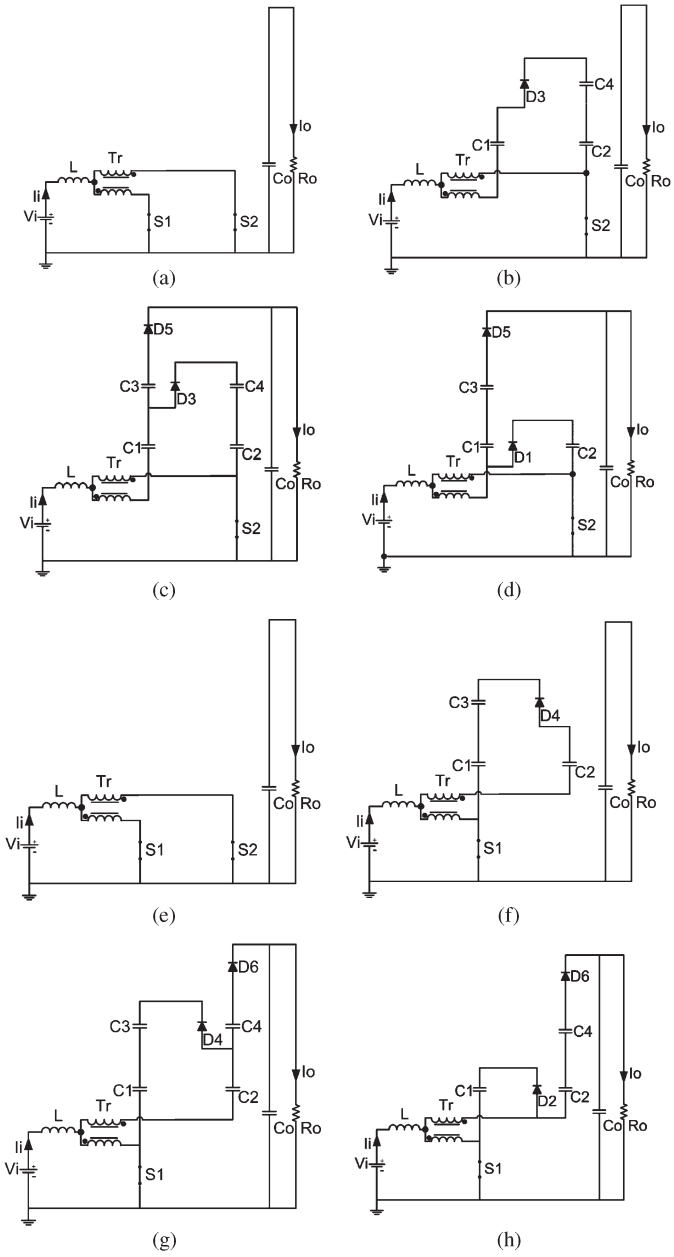


Fig. 3. Operating stages ($mc = 2$). (a) First stage; (b) second stage; (c) third stage; (d) fourth stage; (e) fifth stage; (f) sixth stage; (g) seventh stage; (h) eighth stage.

Eighth stage $[t_7, t_8]$ (Fig. 3(h): This stage is similar to the fourth one, but switch S_1 remains turned on, and switch S_2 remains turned off instead.

$$V_{D5} = V_{D6} = (D-1)\cdot \Delta V_c + \frac{V_o \cdot D}{3} + \left(\frac{2\cdot C_4^2}{C_2} + 12\cdot C_4\right)\cdot \frac{\Delta V_c^2}{T_s \cdot I_L}. \quad (1)$$

2) Static Gain and Energy Storage Elements: The static gain of the converter can be obtained from the inductor volt-second balance. The voltage area multiplied by the time interval that corresponds to the inductor charge is equal to that

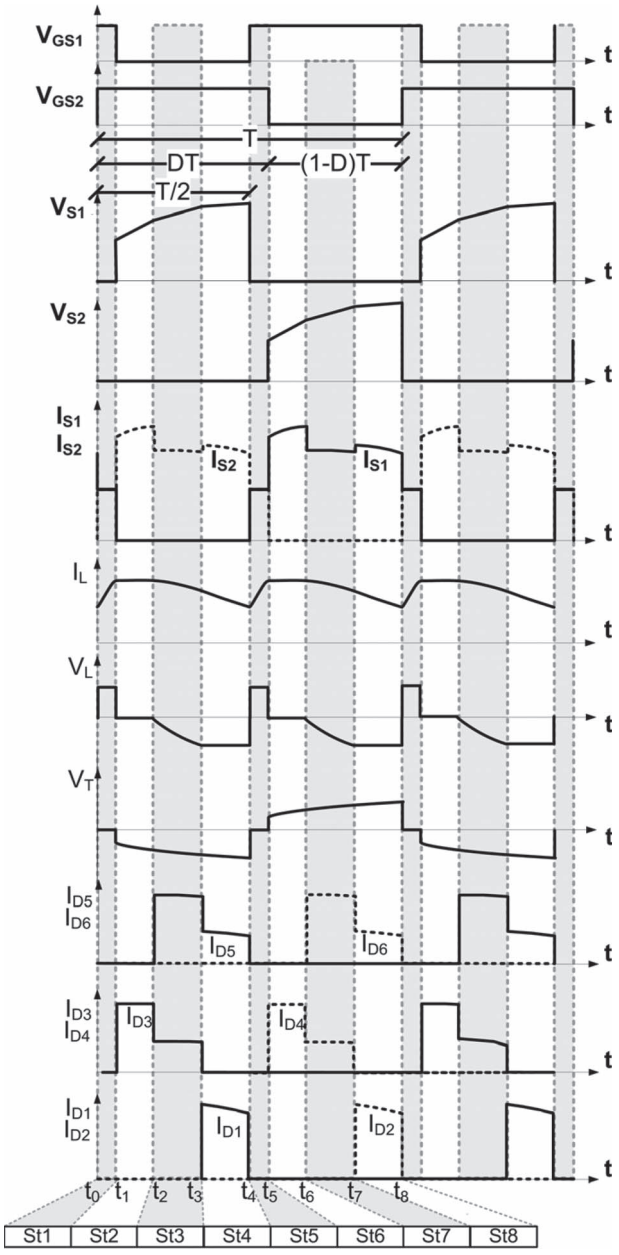


Fig. 4. Main theoretical waveforms ($mc = 2$).

regarding the discharge. The following expressions can then be derived:

$$V_i \cdot \left(D \cdot T_s - \frac{T_s}{2}\right) = -\left(V_i - \frac{V_o}{4}\right) \cdot (1 - D \cdot T_s) \quad (2)$$

$$\frac{V_o}{V_i} = \frac{2}{(1-D)} \quad (3)$$

where V_i is the input voltage.

Expression (3) can then be generalized for any number of VMCs mc as

$$Gv = \frac{V_o}{V_i} = \frac{(mc+1)}{(1-D)}. \quad (4)$$

Expression (4) is plotted and shown in Fig. 5. The dotted line plotted in Fig. 5 corresponds to $1/1 - 2 \cdot D$, representing the

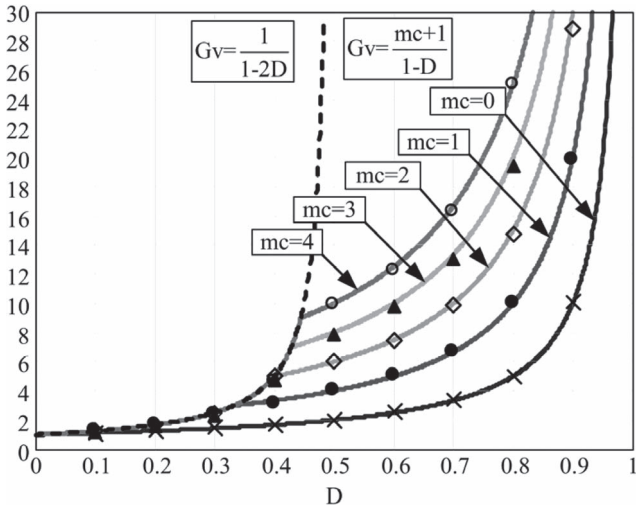


Fig. 5. Static gain curves considering several VMCs.

boundary from which the static gain changes. One can see that it really occurs for $D < 0.5$ at a different point for each number of employed multiplier cells because the multiplier capacitors are not fully charged due to the reduced charge time.

The average values of the output current I_o and output voltage V_o as a function of the duty cycle, input current I_i, input voltage V_i, and number of multiplier cells mc are defined by, respectively,

$$V_o = \frac{V_i \cdot (mc+1)}{(1-D)} \quad (5)$$

$$I_o = \frac{I_i \cdot (1-D)}{(mc+1)}. \quad (6)$$

Assuming that the current through inductor L increases linearly during the first operating stage, what is valid for the generic configuration in Fig. 1, the following expression results

$$L \cdot \frac{\Delta i_L}{\Delta t} = V_i = \frac{V_o \cdot (1-D)}{(mc+1)} \quad (7)$$

where Δi_L is the ripple current through the inductor and Δt is the time interval that corresponds to the overlapping between the drive signals applied to the main switches, determined by (8)

$$\Delta t = \left(D - \frac{1}{2}\right) \cdot T_s = (2 \cdot D - 1) \cdot \frac{T_s}{2} \quad (8)$$

Substituting (8) in (7) gives

$$L \cdot \frac{\Delta i_L}{(2 \cdot D - 1) \cdot \frac{T_s}{2}} = \frac{V_o \cdot (1-D)}{(mc+1)}. \quad (9)$$

By rearranging (9), expression (10) can be obtained, which corresponds to the normalized ripple current β as a function of the duty cycle

$$\beta = \frac{2 \cdot L \cdot \Delta i_L}{T_s \cdot V_o} = \frac{(1-D) \cdot (2 \cdot D - 1)}{(mc+1)}. \quad (10)$$

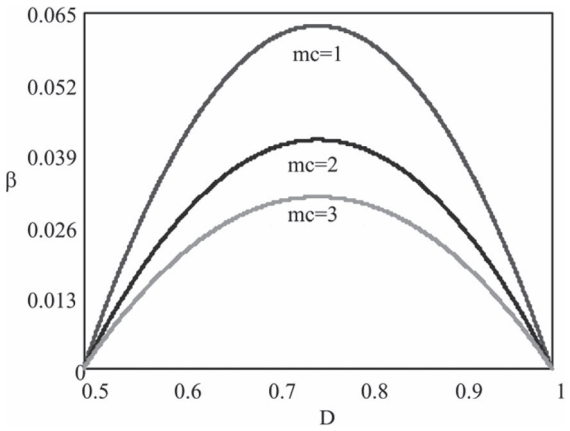


Fig. 6. Normalized ripple current as a function of the duty cycle.

Expression (10) is plotted in Fig. 6, where it can be seen that the maximum ripple current is obtained when $D = 0.75$, and the respective inductance is calculated from

$$L = \frac{V_o}{16 \cdot f_s \cdot (mc + 1) \cdot \Delta I_L}. \tag{11}$$

The multiplier capacitors C_n and the output capacitor C_o can be obtained from the following expressions:

$$C_1{=}C_2{=}\frac{1}{4}\frac{I_i{\cdot}(1{-}D)}{f_s{\cdot}\Delta V_c} \quad \text{if } mc{=}1 \tag{12}$$

$$C_{2j+1}{=}C_{2j+2}{=}\frac{1}{(3{\cdot}n)}\frac{I_i{\cdot}(1{-}D)}{f_s{\cdot}\Delta V_{Cn}} \tag{13}$$

$j{=}0, 1, 2, \ldots$ for $n{=}1, 2, \ldots,$ respectively, if $mc{=}2$

$$C_{2j+1}{=}C_{2j+2}{=}\frac{(3{-}n{+}1)}{8}\frac{I_i{\cdot}(1{-}D)}{f_s{\cdot}\Delta V_{Cn}} \tag{14}$$

$j{=}0, 1, 2, \ldots$ for $n{=}1, 2, 3, \ldots,$ respectively, if $mc{=}3$

$$C_o{=}\frac{I_o{\cdot}(1{-}D)}{2{\cdot}\Delta V_c{\cdot}f_s}. \tag{15}$$

3) Semiconductor Elements: The rms currents through the switches and diodes can be obtained by the following expressions:

$$I_{S1(\mathrm{rms})} = I_{S2(\mathrm{rms})} = \frac{I_L}{12}{\cdot}\sqrt{6 \cdot (11 - 5 \cdot D)} \tag{16}$$

$$I_{D1(\mathrm{rms})} = I_{D2(\mathrm{rms})} = \frac{1}{6} I_L \cdot \sqrt{2 \cdot (1 - D)} \tag{17}$$

$$I_{D3(\mathrm{rms})} = I_{D4(\mathrm{rms})} = \frac{1}{12} I_L \cdot \sqrt{10 \cdot (1 - D)} \tag{18}$$

$$I_{D5(\mathrm{rms})} = I_{D6(\mathrm{rms})} = \frac{1}{12} I_L \cdot \sqrt{6 \cdot (1 - D)} \tag{19}$$

where I_L is the current through boost inductor L.

The average currents through the switches are given by

$$I_{S1(avg)} = I_{S2(\mathrm{avg})} = \frac{1}{6} \cdot (D + 2) \cdot I_L. \tag{20}$$

The average currents through the diodes are given by

$$I_{D1\ldots D6(\mathrm{avg})} = (1 - D) \cdot \frac{1}{6} \cdot I_L. \tag{21}$$

The maximum voltages across the switches and diodes are given by

$$V_{S1} = V_{S2} = \frac{V_o}{3}(1 - D) - \frac{\Delta V_c^2}{I_L \cdot T_s}\left(4 \cdot \frac{C_4^2}{C_2} - 14 \cdot C_4\right) \tag{22}$$

$$V_{D1} = V_{D2} = (1 - D) \cdot \Delta V_c + \frac{V_o}{3} - \left(\frac{4 \cdot C_4^2}{C_2} - 8 \cdot C_4\right) \cdot \frac{\Delta V_c^2}{T_s \cdot I_L} \tag{23}$$

$$V_{D3} = V_{D4} = \frac{V_o}{3} - \left(\frac{2 \cdot C_4^2}{C_2} + 4 \cdot C_4\right) \cdot \frac{\Delta V_c^2}{T_s \cdot I_L} \tag{24}$$

where ΔV_c is the ripple voltage across the multiplier capacitors, T_s is the switching period, and V_o is the output voltage.

4) Autotransformer: The active power processed by the high-frequency autotransformer can be obtained similar to that processed by its low-frequency counterpart, as demonstrated in [30]. In addition, it has been shown that it corresponds to half of the total output power.

The autotransformer can be designed analogously to that of a full-bridge converter [30], while the following expression is valid:

$$A_e \cdot A_w = \frac{\frac{P_o}{2}}{k_t \cdot k_u \cdot k_p \cdot J_{\max} \cdot \Delta B_{\max} \cdot (2 \cdot f_s)} \cdot 10^4 \tag{25}$$

where

A_e is the effective core area,
A_w is the window area,
k_t is the topology factor,
k_u is the utilization factor of the window,
k_p is the utilization factor of the primary winding,
$J_{\max}$ is the maximum current density, and
$B_{\max}$ is the maximum variation of the magnetic flux.

The leakage inductance of the autotransformer is quite small and rated at the order of some μH. The windings are symmetrically displaced in the core, i.e., with the same number of turns and parallel-connected wires. The impact of the leakage inductance in the static gain is negligible, as it will be demonstrated by the experimental results. The energy stored in the leakage inductance flows through the multiplier cells and the transfer diodes, while the peak voltages across the main switches are reduced even when snubbers are not used. The autotransformer is designed according to guidelines used in conventional high-frequency counterparts, with the same typical values used to represent the magnetizing inductance. The currents through the windings are balanced, and the number of turns does not compromise the converter efficiency significantly.

TABLE I
DESIGN SPECIFICATIONS FOR THE STEP-UP CONVERTERS

Parameter	Specification
Rated output power	P_o=1000 W
Minimum input voltage	$V_{i(min)}$=42 V
Maximum input voltage	$V_{i(max)}$=54 V
Rated input voltage	V_i=48 V
Output voltage	V_o=400 V
Switching frequency	f_s=25 kHz
Ripple current through inductor L	ΔI_L=15%·I_{imax}
Ripple voltage through multiplier capacitors $C_1 \ldots C_6$	ΔV_{Ck}=8.75%·V_o
Ripple voltage through output capacitor C_o	ΔV_{Co}=5%·V_o
Expected theoretical efficiency	η=95%
Autotransformer turns ratio	n=1

TABLE II
SPECIFICATIONS OF A CONVENTIONAL BOOST CONVERTER

Component	Specifications
	***mc*=2**
Inductor L	Two cores are used. Core type: 2×NEE 0P49928EC (100×59×27 mm) Inductance: 4.5 mH Wire: 8×AWG19
Switches S	IGBT IRG4PC40KDPBF (600 V, 25 A@100 °C)
Diodes $D_1 \ldots D_8$	Ultra fast diode HFA25PB60
Output capacitor C_o	4.4 μF /400 V

III. THEORETICAL COMPARISON WITH THE CONVENTIONAL BOOST CONVERTER

As it was mentioned before, the traditional boost converter may not be suitable for applications with high conversion ratio because extreme values for the duty cycle are required. In addition, if the duty cycle is too high, conventional drive circuits become inadequate. As a practical matter, it is reasonable to assume that the input voltage can be increased up to three or four times in a boost converter.

The proposed approach is based on the use of VMCs to further increase the step-up ability of the boost converter. Let us establish a theoretical comparison between both structures by initially considering the parameter set given in Table I.

Table I shows that the conversion ratio may be higher than nine if the minimum input voltage is considered. The inductance of the filter inductor in the classical boost topology is proportional to the rated duty cycle. In addition, the size of such magnetic element depends on the input current rating. If the parameters given in Table I are used, a boost converter can be designed with the specifications provided in Table II.

First, it is important to notice in Table II that the filter inductor is so large that it is split into two cores. Second, the high current and voltage stress regarding the active switch do not allow the use of a single semiconductor element if MOSFETs are considered. If the association of MOSFETS in parallel and/or in series is not desired, the use of insulated gate bipolar transistors (IGBTs) is a must.

The loss mechanism in the arrangement specified in Table II is of major concern. Poor efficiency is expected over the entire load range due to appreciable loss in the inductor and the main switch. All losses involving the semiconductor elements and the inductor were then calculated for the output power ranging between 100 and 1000 W, and the results are presented in Fig. 7. It can be seen that efficiency is about 88% at light load, but it drops heavily at rated load (75.8%). It can be explained because

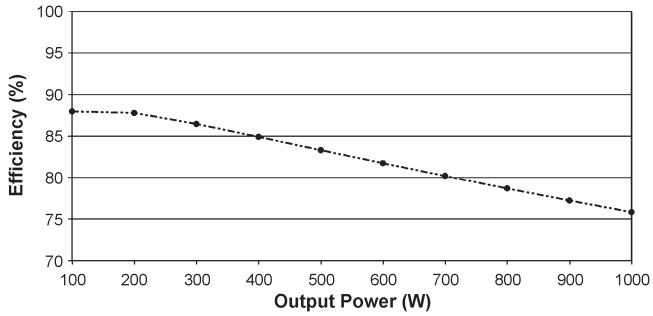
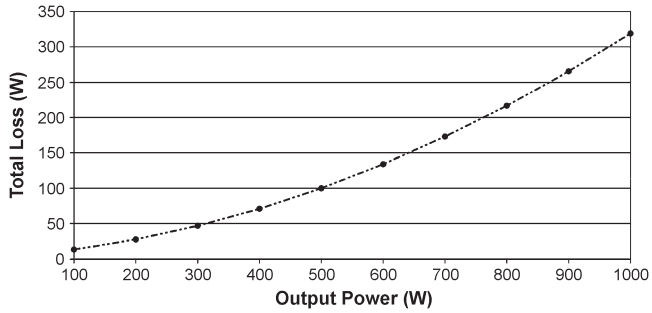
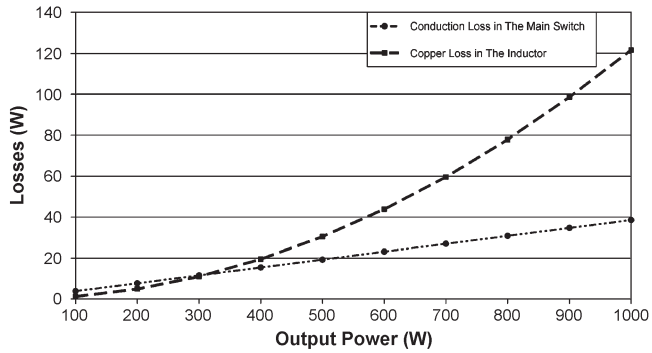


Fig. 7. Theoretical efficiency curve of the conventional boost converter.



(a)



(b)

Fig. 8. Profile of losses in the boost converter. (a) Total loss. (b) Conduction loss in the IGBT switch and copper loss in the filter inductor.

the major sources of losses are the boost inductor and the IGBT. It is important to remember that copper losses are proportional to the square of the current. In order to validate this assumption, the total loss is shown in Fig. 8(a), whose curve is nearly parabolic. Its shape is mainly influenced by the profile of the copper loss in the inductor, which is represented in Fig. 8(b). If MOSFET switches were used, the curve in Fig. 8(a) would tend to a more parabolic shape, further reducing the efficiency at heavy load.

Based on the aforementioned results, some important questions can be raised. Of course, the operating frequency in the classical boost converter is equal to the switching frequency. The inductor is designed for twice the switching frequency in the proposed converter, with significant reduction of size, weight, and volume. By comparing Tables II and III, it can be seen that the volume of the filter inductor is significantly reduced in the introduced approach. However, the autotransformer and additional components such as multiplier capacitors and diodes must be considered in terms of the overall volume. As a general conservative estimate, it can be considered that the

TABLE III
SPECIFICATIONS OF THE 3SSC-BASED BOOST CONVERTER

Component	Specifications
	***mc*=2**
Inductor L	Toroidal core: Magnetics 58195A2 Inductance: 70 μH Turns ratio: 22 Wire: 55×AWG 26
Autotransformer T_r	Core: Thornton NEE-65/33/26 Primary turns: 19 Primary winding: 28×AWG 26 Secondary turns: 19 Secondary winding: 28×AWG 26
Switches S_1 and S_2	MOSFET IRFP4227
Diodes D_1… D_8	Ultra fast diode HFA25PB60
Capacitors C_1 and C_2	Epcos B32594, 2×2.2 μF / 400 V
Capacitors C_3 and C_4	Epcos B32594, 1×2.2 μF / 400 V
Output capacitor C_o	Epcos B43304, 680 μF / 450 V

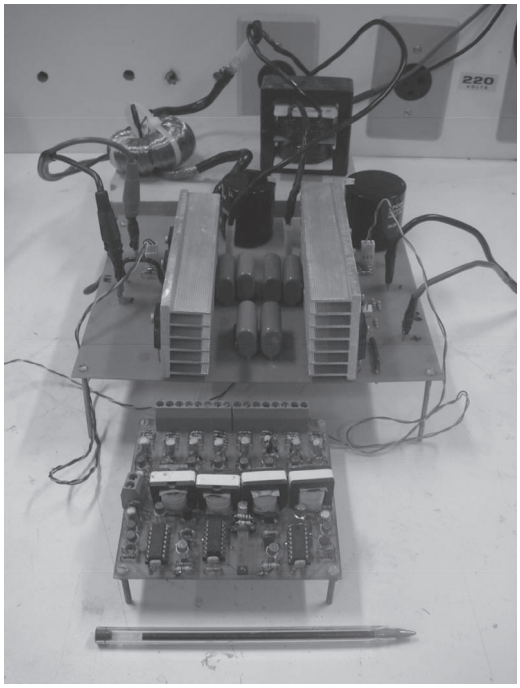


Fig. 9. Photograph representing the experimental prototype.

weight and volume of magnetics for both converters are pretty much the same.

However, efficiency tends to be a serious drawback of the conventional boost converter if large conversion ratios are considered. The theoretical example presented in this section is not practical, but it intends to clearly show that the proposed converter is feasible for high-current high-voltage step-up applications. On the other hand, if low conversion ratios are considered, the traditional boost topology becomes more attractive, mainly due to the high component count of the 3SSC-based converter.

IV. EXPERIMENTAL RESULTS

An experimental prototype for the structure with two multiplier cells has been designed according to the previous guidelines and implemented in laboratory. Preliminary specifications are given in Table I, while the components used in the prototype are listed in Table III and a picture is shown in Fig. 9.

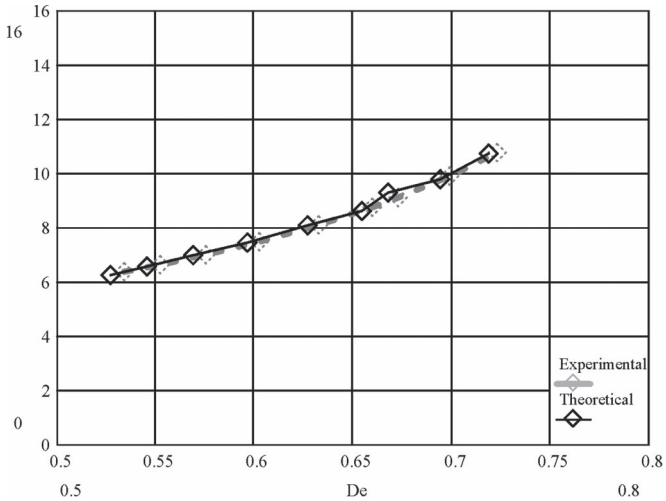


Fig. 10. Comparison between the theoretical and experimental curves for the static gain.

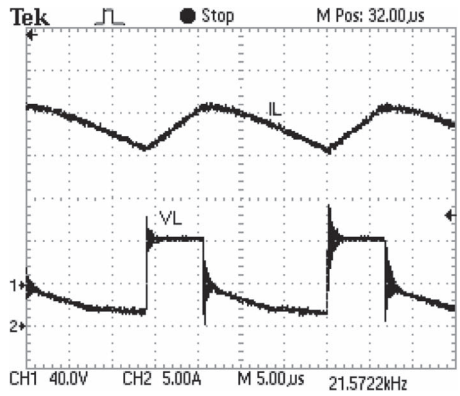


Fig. 11. Current (I_L – CH1) and voltage (V_L – CH2) waveforms for inductor L.

The converter was evaluated by varying the duty cycle, while the ratio between the output voltage and the output voltage was measured. Fig. 10 presents the comparison between the theoretical and experimental curves of the static gain, which are nearly the same.

Fig. 11 shows the waveforms regarding inductor L, where it can be seen that the ripple current is 6 A. The voltage across the inductor varies from -30 to $+42$ V. The voltage is constant when both switches are turned on, and its average value is null.

The currents through both windings of the autotransformer with unity turns ratio are shown in Fig. 12. It is expected that the current is equally shared in two halves of the current through inductor L. Small unbalance exists between the currents because there is as slight difference of 130 ns observed in the width of the gating pulses applied to the main switches and intrinsic nonidealities. The ripple current in Fig. 12 is approximately 2.5 A. The peak voltage across each winding is equal to half that through the switch and varies from -76 to $+76$ V. In addition, the average voltage across each winding is null.

Fig. 13 represents the commutation of switches S_1 and S_2. The voltages across the switches are approximately the same, although 180° displaced. The maximum voltages across the switches are 160 V, which is a value close to the theoretical calculation. It can be seen that the voltage across the switch is

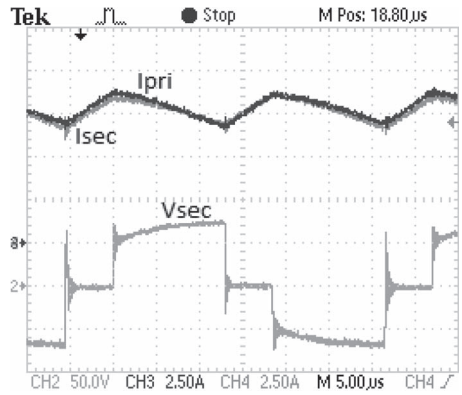


Fig. 12. Currents through the primary ($I_{\rm pri}-$ CH3) and secondary windings ($I_{\rm sec}-$ CH4) and voltage across the primary winding of the autotransformer ($V_{\rm sec}-$ CH2).

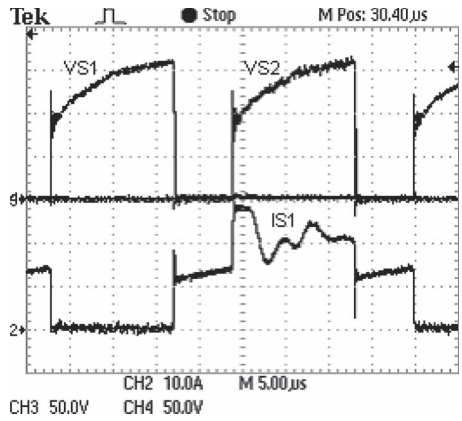


Fig. 13. Drain-to-source voltage across switch $S_1(V_{S1}-$ CH3), drain-to-source voltage across switch $S_2(V_{S2}-$ CH4), and current through switch $S_1(I_{S1}-$ CH2).

lower at the beginning of the turning-off process. The current through switch S_1 is discontinuous due to the commutation of the multiplier diodes, as predicted in the theoretical analysis. In addition, the current peak is equal to the inductor current, i.e., 30 A. Some oscillation occurs in the current through switch S_1 when switch S_2 is turned off due to the intrinsic capacitance of the switches and the transformer leakage inductance, but it is not supposed to influence the converter performance significantly. Even though the leakage inductance of the autotransformer has not been considered in the analysis, it is not supposed to influence the commutation because the currents through the switches have reduced di/dt rates.

Fig. 14 shows the detailed commutation of switch S_1, and it is expected that switching losses during turn on become reduced when higher number of multiplier stages is used, as demonstrated in [7]. Fig. 15 also presents the behavior of the switching loss during turn off, while improved performance is also expected for topologies with more than two cells. The experimental results in Fig. 14 are very close to the theoretical waveforms presented in Fig. 4, but small oscillations during the seventh and eight stages occur in the loop formed by the multiplier capacitors and transformer leakage inductance.

Fig. 16(a) shows the voltages across the multiplier diodes D_1, D_3, and D_5. It is worth to mention that those waveforms

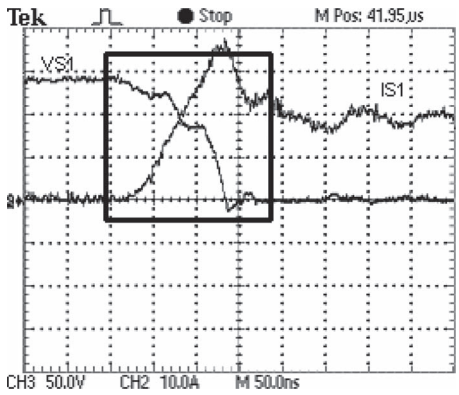


Fig. 14. Switching detail during turn on ($I_{S1}-$ CH2, $V_{S1}-$ CH3).

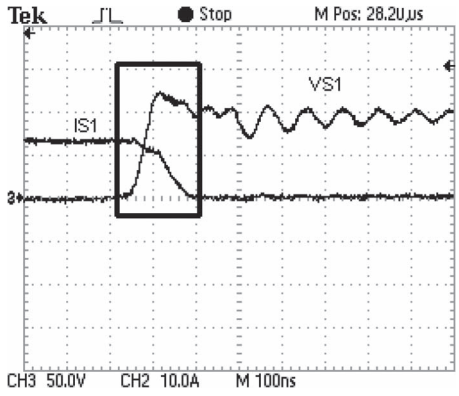


Fig. 15. Switching detail during turn off ($I_{S1}-$ CH2, $V_{S1}-$ CH3).

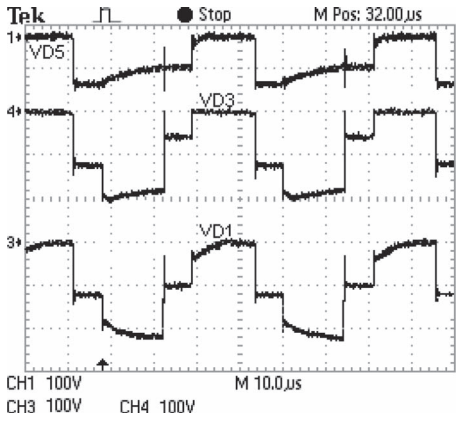


Fig. 16. Voltages across the multiplier diodes ($V_{D1}-$ CH3, $V_{D3}-$ CH4, $V_{D5}-$ CH1).

regarding diodes D_2, D_4, and D_6 are similar, but 180° displaced. The voltages across diodes D_1 and D_2 for the first multiplier level are higher than 200 V due to the sum of the voltages across the switches and adjacent capacitors. However, the voltages across diodes D_5 and D_6 are approximately 140 V because there are no adjacent capacitors.

The voltages across multiplier capacitors C_2 and C_4 are shown in Fig. 17, which are nearly the same. In addition, the ripple voltage across the capacitors is the same for the multiplier capacitors, according to Table I.

Fig. 18 represents the waveforms regarding the input voltage, output voltage, and output current, which assume values

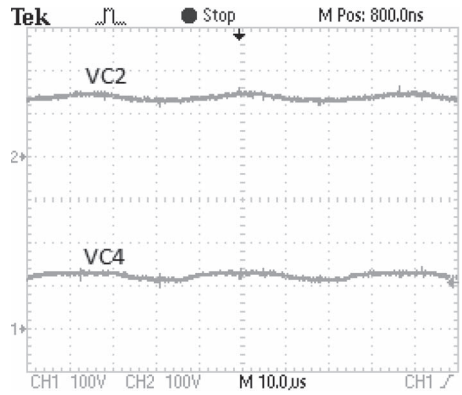


Fig. 17. Voltage across multiplier capacitors $C_2(V_{C1} - \text{CH1})$ and $C_4(V_{C4} - \text{CH2})$.

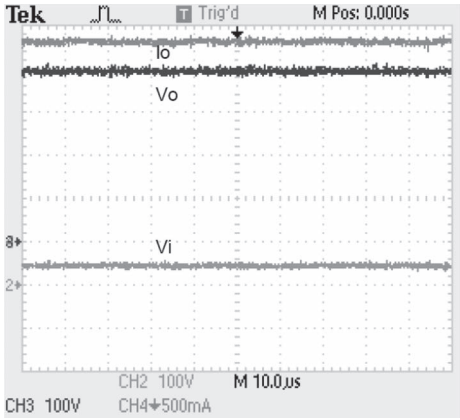


Fig. 18. Output current $(I_o - \text{CH4})$, output voltage $(V_o - \text{CH3})$ waveforms in steady state when $V_i = 48$ V$(V_i - \text{CH2})$.

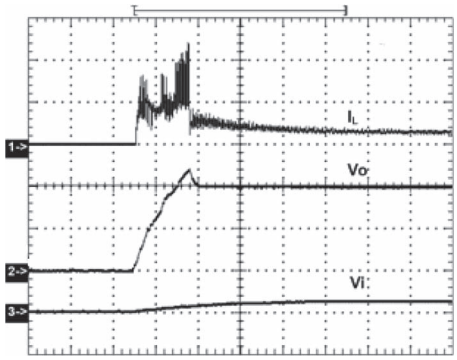


Fig. 19. Inductor current $(I_L - \text{CH1})$, output voltage $(V_o - \text{CH2})$, and input voltage $(V_i - \text{CH3})$ waveforms during startup.

according to the specifications given in Table I. It can be seen that the performance of the designed controllers in closed-loop operation is satisfactory.

The converter modeling and design guidelines regarding the control system are presented in [31] and will not be discussed here again. The converter startup is shown in Fig. 19, where the output voltage reaches 400 V as desired, and the input voltage increases from null to 48 V. Voltage overshoot equal to 80 V is verified during the process, mainly because the capacitors are initially discharged and behave as a short circuit. Output voltage regulation begins when the input voltage equals 20 V.

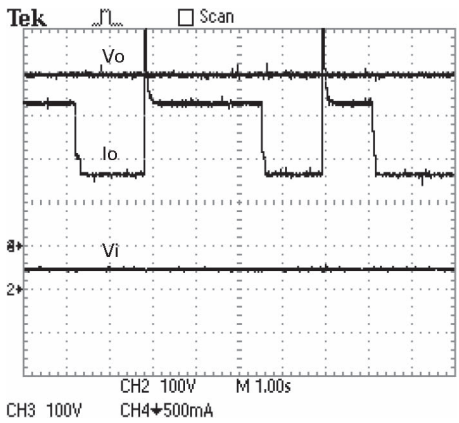


Fig. 20. Output current $(I_o - \text{Ch4})$, output voltage $(V_o - \text{CH3})$, and input voltage $(V_i - \text{CH2})$ behavior during load step disturbance.

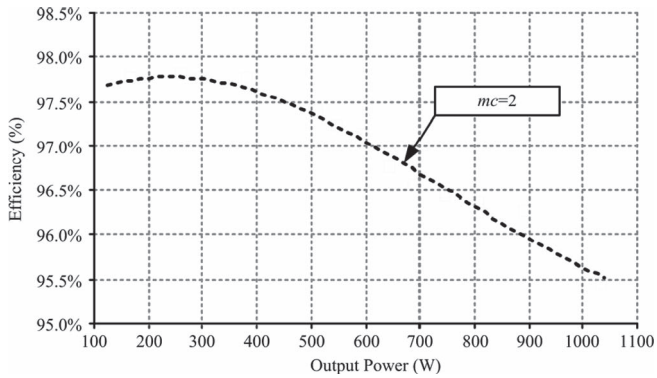


Fig. 21. Efficiency as a function of the output power.

Fig. 20 shows the behavior of the converter during load steps. While the output current increases or decreases significantly, the input voltage and the output voltage remain constant and insensitive to the disturbances. Current overshoot occurs during the load step because incandescent lamps were used in the tests, which on the other hand, present reduced impedance when cold. Thus, the load current tends to increase, as its peak value reaches twice or even three times the rated value, although this does not occur at negative load step.

Finally, the efficiency curve of the topology designed according to the conditions in Tables I and III is shown in Fig. 21. High efficiency results for the entire load range, while the maximum value is 97.7% and higher than 95.5% at rated power. Since MOSFETs were used in the prototype, and they present appreciable on-resistance, conduction losses regarding the main switches become proportional to the square of the drain current. In addition, copper losses are also given by I^2R. Then, the parabolic shape of the curve is expected, while efficiency tends to be reduced at heavy load. However, as it was mentioned before, good performance of the converter is achieved.

V. Conclusion

This paper has proposed a new generalized nonisolated boost converter with high voltage gain. The topology is adequate for several applications such as photovoltaic systems and UPSs, where high voltage gain between the input and output voltages is demanded.

An important characteristic that can be seen in the experimental results is the reduced blocking voltages across the controlled switches compared to similar circuits, allowing the utilization of MOSFETs with reduced on-resistance.

The qualitative analysis, theoretical analysis, and experimental results for a 1-kW prototype have been discussed. The converter achieves good efficiency if compared to similar configurations that were previously proposed in literature. One of the main advantages of the topology lies in the reduced switching losses, because the voltage is nearly null at the initial turn-off instant. In addition, the converter aggregates all the advantages that are intrinsic to topologies based on the 3SSC, that are:

- reduced size, weight, and volume of magnetics, which are designed for twice the switching frequency;
- the current stress through each main switch is equal to half of the total output current, allowing the use of switches with lower current rating;
- losses are distributed among the semiconductors, leading to better heat distribution and consequently more efficient use of the heat sinks;
- energy is transferred from the source to the load during most part of the switching period, which is a distinct characteristic of the proposed converter, since in other boost-type converters it only occurs during half of the switching period. As a consequence, reduction of current peaks and also conduction losses are expected,
- the drive circuit of the main switches becomes less complex because they are connected to the same reference node.

ACKNOWLEDGMENT

The authors gratefully acknowledge CNPq, CAPES, FAPEMIG, and FUNCAP for the support to this work, and also "CM Comandos Lineares Ltda" for supplying samples.

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