DC-AC POWER SUPPLY FOR BATTERY BASED SYSTEMS

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***Abstract* – This work presents the analysis, design, and experimental development of a single-phase inverter with high frequency transformer isolation and for a wide input voltage range. The high frequency input current ripple is mitigated by the use of a small input LC filter, and the low frequency current component injected by the inverter is attenuated by the voltage loop controller. The proposed topology can be used in dc voltage-sourced applications such as renewable energy and battery based systems.**

***Keywords* – dc-ac conversion, high frequency isolation, wide input voltage range operation.**

I. INTRODUCTION

The dc-ac converters are particularly one of the most significant and studied class of static power converters. Typical applications are distributed generation, ac motor drives, and battery based systems. Several topologies are available in the literature, which can be classified according to the following characteristics [1]:

- Number of phases: single-phase or three-phase;
- Adjustment of the output voltage;
- Commutation of the switches: hard or soft;
- Presence or absence of isolation transformer;
- Number of power stages.

This work describes the analysis, design, and experimental results of a dc-ac converter that has characteristics such as: single-phase, adjustment of the output voltage, hard commutation of the switches, and high frequency isolation, applied in the implementation of a 400VA, 220Vrms, and 400Hz power source from a 60-90Vdc battery input voltage. This equipment is currently operating in the trains of the FEPASA (Ferrovia Paulista S.A., Brazil).

A. Single-Stage Topologies vs. Mutiple-Stage Topologies

DC-AC converters can be classified in either single-stage or multiple-stage topologies. A single-stage dc-ac converter [2]-[11] is that one that has only one power processing stage, responsible not only for the output voltage adjustment, but also for the sine modulation of the output voltage. A typical example is the dual flyback inverter [7], shown in Figure 1.

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A multiple-stage dc-ac converter is formed by several converters where each one has a specific function, e.g. output voltage adjustment and/or isolation and/or dc-ac conversion. They can be classified in three types: dc-ac-ac converters [12]-[13] (Figure 2), dc-dc-ac converters [14]-[20] (Figure 3), or dc-ac-dc-ac converters (Figure 4).

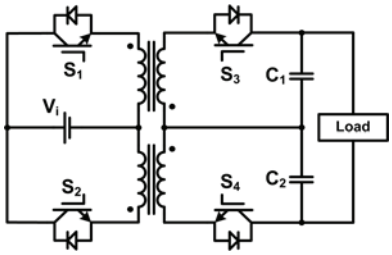

Fig. 1. Dual flyback inverter.

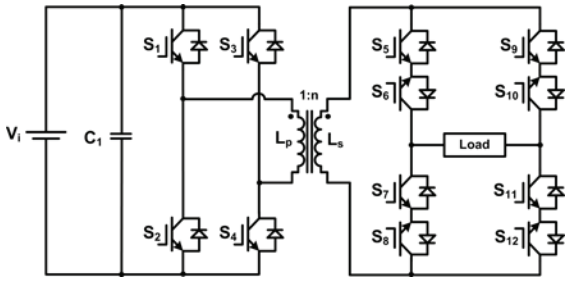

Fig. 2 Example of a dc-ac-ac topology.

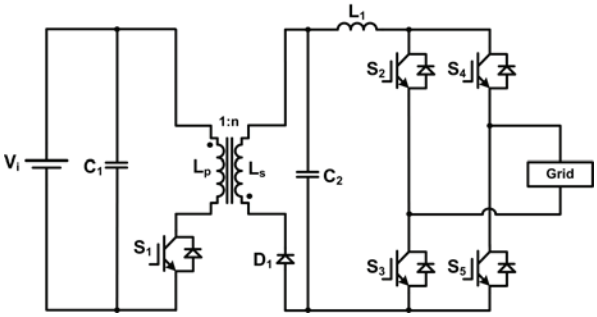

Fig. 3 Example of a dc-dc-ac topology.

Single-stage dc-ac converters are typically used in low power applications [1]. Multiple-stage dc-ac-ac converters possess one high number of semiconductors, reducing the efficiency and increasing the cost. Multiple-stage dc-dc-ac converters have output in current, are applied in grid connected systems. Therefore, these topologies are not the scope of this work, which is focused on dc-ac-dc-ac structures.

II. PROPOSED TOPOLOGY

Figure 4 shows the block diagram representing a dc-ac-dc-ac system. It is formed by three power stages, as each one of them can be implemented using a classical topology. One is supposed to define which structures must be employed.

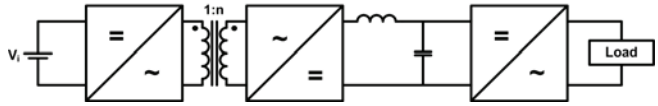

Fig. 4 Block diagram of a dc-ac-dc-ac system.

The complete schematic of proposed topology is shown in Figure 5.

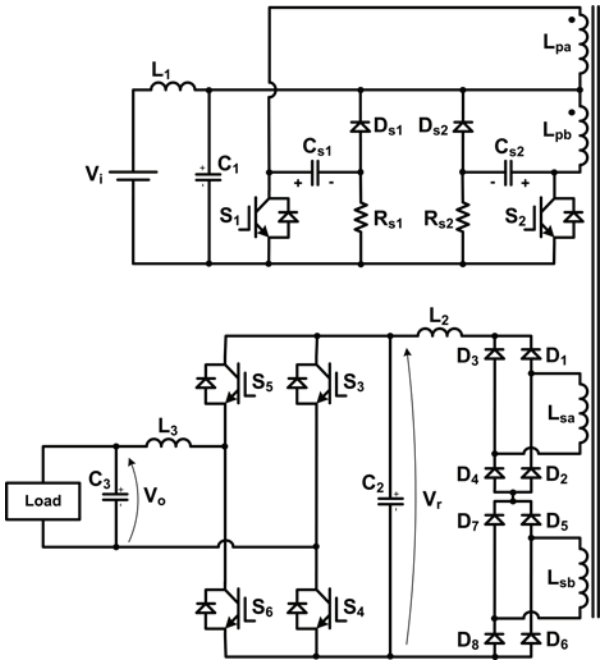

Fig. 5 Proposed topology.

A classical push-pull converter is used in the first stage, because the switches are not turned on simultaneously, and also due to the intrinsic isolation.

A full-bridge rectifier is chosen in the second stage, due to the absence of central tap and the reduced blocking voltage across the diodes. To further reduce the blocking voltage, two secondary windings are employed in the transformer of the push-pull converter.

The third stage is composed by a full-bridge inverter, once that a push-pull arrangement would require an additional low frequency transformer. A half-bridge topology is not adequate as well, due to the doubled input voltage.

Three LC filters are employed. The first one is placed between the primary voltage source and the first stage, in order to assure reduced high frequency ripple of the input current. The second one is placed between the second and third stages, to provide the dc voltage link to the full-bridge inverter and also mitigate high frequency current flow through the previous stages. The last filter is placed in the load side.

A dissipative RCD snubber is employed in the switches of the push-pull converter to preserve the semiconductor devices due to eventual voltage overshoot caused by the leakage inductance of the high frequency transformer.

III. DESIGN PROCEDURE

The prototype specifications and design assumptions are shown in Table I.

TABLE I
Prototype Specifications and Design Assumptions

Parameter	Specification
Input voltage range	V_i=60-90V
Rms output voltage	V_o=220V_{rms} +/-5%
Maximum output voltage THD	<5%
Apparent power	S_o=400VA
Load power factor	PF=1
Output fundamental frequency	f_r=400Hz
Modulation index	Ma=0.75
Maximum input current ripple	ΔI_i=6%
Maximum input voltage ripple	ΔV_i=3V
Efficiency (push-pull converter)	η_1=0.9
Efficiency (full-bridge converter)	η_2=0.9
Switching frequency (push-pull converter)	f_1=40kHz
Switching frequency (full-bridge converter)	f_2=40kHz

A. Power Circuit Design

The peak value of output voltage (V_{o_pk}) is given by (1).

$$V_{o\_pk} = \sqrt{2} \cdot V_o \rightarrow V_{o\_pk} \cong 311V \quad (1)$$

The input voltage of third stage (V_r) is given by (2).

$$V_r = \frac{V_{o\_pk}}{M_a} \rightarrow V_r \cong 420V \quad (2)$$

Considering the maximum duty cycle in the push-pulll converter equal to 0.45, the minimum turns ratio (n) is given by (3).

$$n > \frac{V_r}{2 \cdot D_{\max} \cdot V_{i\_\min}} \rightarrow n > 7.78 \quad (3)$$

By convenience, the transformer turns ratio is chosen:

$$n = 8 \quad (4)$$

Thus the minimum duty cycle (D_{min}) in the push-pull converter is given by (5).

$$D_{\min} = \frac{V_r}{2 \cdot n \cdot V_{i\_\max}} \rightarrow D_{\min} \cong 0.29 \quad (5)$$

The peak current drained by the push-pull converter is given by (6).

$$I_{sh\_pk} = \frac{S_o \cdot PF \cdot n}{\eta_1 \cdot \eta_2 \cdot V_r} \rightarrow I_{sh\_pk} \cong 9.52A \quad (6)$$

The maximum and minimum average currents through the primary voltage source (I_{i_max} and I_{i_min}, respectively) are given by (7) and (8), respectively.

$$I_{i\_\max} = \frac{S_o \cdot PF}{\eta_1 \cdot \eta_2 \cdot V_{i\_\min}} \rightarrow I_{i\_\max} \cong 8.33A \quad (7)$$

$$I_{i\_\min} = \frac{S_o \cdot PF}{\eta_1 \cdot \eta_2 \cdot V_{i\_\max}} \rightarrow I_{i\_\min} \cong 5.56A \quad (8)$$

The rms current through filter capacitor C_1 is given by (9).

$$I_{C1\_rms} = I_{sh\_pk} \cdot \sqrt{2 \cdot D_{\min} \cdot (1 - 2 \cdot D_{\min})} \rightarrow I_{C1\_rms} \cong 4.7A \quad (9)$$

The maximum equivalent series resistance of capacitor C_1 (R_{C1}) is given by (10).

$$R_{C1} < \frac{\Delta V_i}{I_{sh\_pk}} \rightarrow R_{C1} < 315m\Omega \quad (10)$$

The filter inductance (L_1) is given by (11).

$$L_1 = \frac{\Delta V_i \cdot D_{\max}}{\Delta I_i \cdot I_{i\_\min} \cdot f_1} \rightarrow L_1 = 100\mu H \quad (11)$$

The rms value current through capacitor C_2 is obtained by simulation and given by (12).

$$I_{C2\_rms} \cong 2A \quad (12)$$

The peak output current (I_{o_pk}) is given by (13).

$$I_{o\_pk} = \sqrt{2} \cdot \frac{S_o \cdot PF}{V_o} \quad (13)$$

Considering the voltage ripple across C_2 as 1% of V_r, the maximum equivalent series resistance of C_2 (R_{C2}) is given by (14).

$$R_{C2} < \frac{0.01 \cdot V_r}{I_{o\_pk}} \rightarrow R_{C2} < 1.6\Omega \quad (14)$$

The cut-off frequency of the second filter (f_{f2}) must be established so that the components from 800Hz the input current inverter are blocked and allow a reasonable inductor filter size. For the given example this frequency is defined as 110Hz and then inductance L_2 is given by (15).

$$L_2 = \frac{1}{(2 \cdot \pi \cdot f_{f2})^2 \cdot C_2} \rightarrow L_2 = 21mH \quad (15)$$

Considering the current ripple through inductor L_3 as 35% of I_{o_pk}, the respective inductance is given by (16).

$$L_3 = \frac{(V_r - \sqrt{2} \cdot V_o) \cdot M_a}{0.35 \cdot I_{o\_pk}} \rightarrow L_3 = 2.27mH \quad (16)$$

In order to get a cut-off frequency around 4kHz in the third filter, filter capacitance C_3 can be obtained from (17).

$$C_3 = \frac{1}{(2 \cdot \pi \cdot f_{f3})^2 \cdot L_3} \rightarrow C_3 \cong 700nF \quad (17)$$

Table II lists the components used in the prototype.

TABLE II
Components List

Reference	Component
C_1	470uF/250Vdc
C_2	100uF/450Vdc
C_3	1uF/250Vac
C_{s1} and C_{s2}	1nF/400Vdc
D_{s1} and D_{s2}	MUR240
D_1 to D_6	MUR1100
L_1	100µH/8.5A
L_2	21mH/1.1A
L_3	2.27mH/1.8A
R_{s1} and R_{s2}	100Ω/3W
S_1 and S_2	IRFP460A
S_3 to S_6	IRGB20B60PD1

B. DC-AC-DC Control Loop Design

The dc-ac-dc converter can be modeled by a buck converter, as shown in Figure 6.

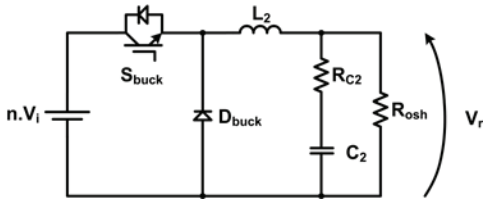

Fig. 6 Equivalent circuit modeling of the dc-ac-dc converter.

The transfer function (TF) of the dc-ac-dc converter is shown in (18) and its Bode diagram is shown in Figure 7.

$$G_{sh}(s) = k_d \cdot \frac{s + \frac{1}{\omega_{zsh}}}{\frac{1}{\omega_{osh}^2} \cdot s^2 + \frac{1}{\omega_{osh} \cdot Q_{sh}} \cdot s + 1} \quad (18)$$

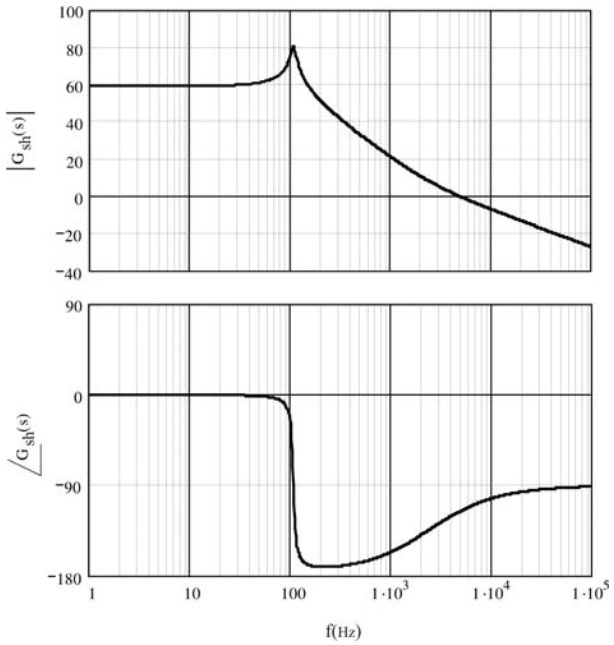

Fig. 7 Bode diagram of Gsh(s).

Where,

$$K_d = n \cdot V_{i\_\max} \rightarrow K_d = 720 \quad (19)$$

$$\omega_{zsh} = \frac{1}{C_2 \cdot R_{C2}} \rightarrow \omega_{zsh} = 14930 \quad rad/s \quad (20)$$

$$\omega_{osh} = \frac{1}{\sqrt{L_2 \cdot C_2}} \cdot \sqrt{\frac{R_{osh}}{R_{osh} + R_{C2}}} \rightarrow \omega_{osh} = 673.64 \quad rad/s \quad (21)$$

$$R_{osh} = \frac{V_r \cdot \eta_2}{P_o} \rightarrow R_{osh} = 400\Omega \quad (22)$$

$$Q_{sh} = \frac{\sqrt{L_2 \cdot C_2 \cdot R_{osh} \cdot (R_{osh} + R_{C2})}}{C_2 \cdot R_{osh} \cdot R_{C2} + L_2} \rightarrow Q_{sh} = 12.17 \quad (23)$$

The open loop TF $G_{sh}(s)$ is given by (24).

$$FTLA_{sh}(s) = G_{sh}(s) \cdot F_m \cdot H_{sh}(s) \quad (24)$$

Where $H_{sh}(s)$ is the feedback TF and F_m is the modulator gain:

$$H_{sh}(s) = \frac{V_{ref}}{V_r} \rightarrow H(s) = 5.95 \times 10^{-3} \quad (25)$$

$$F_m = \frac{1}{V_{ref}} \rightarrow F_m = 0.4 \quad (26)$$

As the control goals are null steady state error and the mitigation of the low frequency ripple of the current through the inverter, a simple PID controller, shown in Figure 8, can be used.

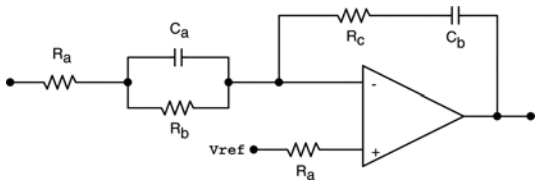

Fig. 8 DC-AC-DC controller.

The zeros of the controller match with the poles of the system, the pole in ω_{zsh} of the controller match with the zero of the system, and an additional pole added at the origin establishes null error in the steady state. The dc-ac-dc converter controller TF is given by (27).

$$C_{sh}(s) = K_{vsh} \cdot \frac{(s + \omega_{osh}) \cdot (s + \omega_{osh})}{s \cdot (s + \omega_{zsh})} \quad (27)$$

The gain K_{vsh} must establish a crossing frequency (f_{csh}) about 150Hz, in order to attenuate the 800Hz current ripple. Then, the K_{vsh} value é dado by (28).

$$K_{vsh} = \frac{1}{FTLA_{sh}(2 \cdot \pi \cdot f_{csh}) \cdot T_{sh}(2 \cdot \pi \cdot f_{csh})} \quad (28)$$

Where,

$$T_{sh}(s) = \frac{(s + \omega_{osh}) \cdot (s + \omega_{osh})}{s \cdot (s + \omega_{zsh})} \quad (29)$$

Then,

$$K_{vsh} = 5.6 \quad (30)$$

Deciding the value of the R_a in 1kΩ, the controller components can be obtained from expressions (31) to (34).

$$R_c = K_{vsh} \cdot R_a \rightarrow R_c = 5.6k\Omega \quad (31)$$

$$C_b = \frac{1}{\omega_{osh} \cdot R_c} \rightarrow C_b = 270nF \quad (32)$$

$$R_b = R_a \cdot \left(\frac{\omega_{zsh}}{\omega_{osh}} - 1 \right) \rightarrow R_b = 22k\Omega \quad (33)$$

$$C_a = \frac{1}{\omega_{osh} \cdot R_b} \rightarrow C_a = 68nF \quad (34)$$

The Bode diagram of the resulting transfer function of the compensated system is shown in Figure 9.

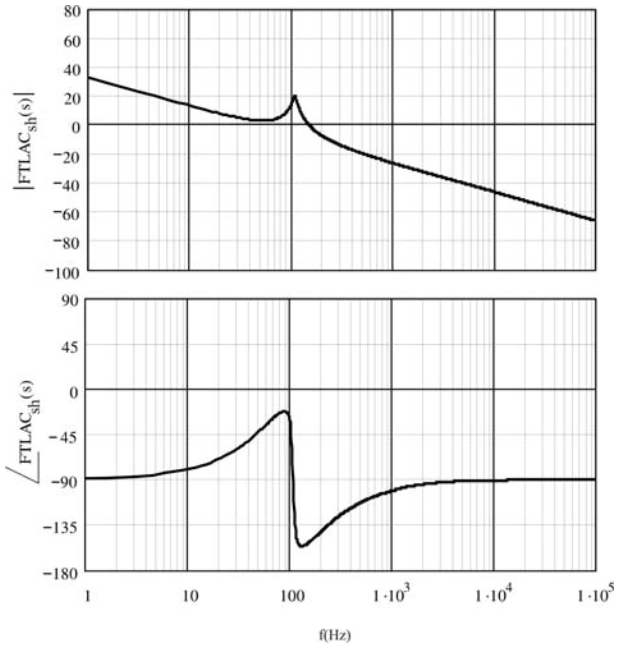

Fig. 9 Bode diagram of FTLACsh(s).

Figure 10 shows the block diagram of the dc-ac-dc stage control.

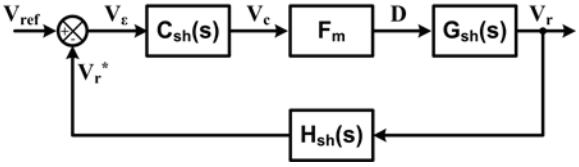

Fig. 10 Block diagram of he dc-ac-dc control.

C. Inverter Control Loop Design

The TF of the dc-ac converter is given by (35).

$$G_{fb}(s) = V_r \cdot \frac{1}{L_3 \cdot C_3 \cdot s^2 + \frac{L_3}{R_o} \cdot s + 1} \tag{35}$$

Where, nominal output resistance (R_o) of the inverter is give by (36).

$$R_o = \frac{V_o^2}{S_o \cdot PF} \tag{36}$$

The feedback gain and the modulator gain are given by (37) and (38), respectively.

$$H_{fb}(s) = \frac{1}{100} \tag{37}$$

$$F_m = \frac{1}{V_{ref}} \rightarrow F_m = 0.4 \tag{38}$$

The open loop TF of the $G_{fb}(s)$ is given by (39).

$$FTLA_{fb}(s) = G_{fb}(s) \cdot F_m \cdot H_{fb}(s) \tag{39}$$

The Bode diagram of the $FTLA_{fb}(s)$ is shown in Figure 11.

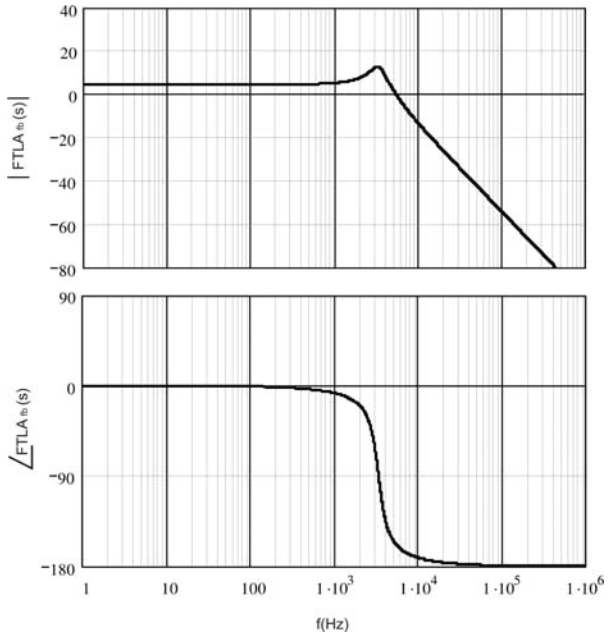

Fig. 11 Bode diagram of FTLAfb(s).

As the control goals are null steady state error and to assure one high speed response, the PID controller shown in Figure 12 can be used.

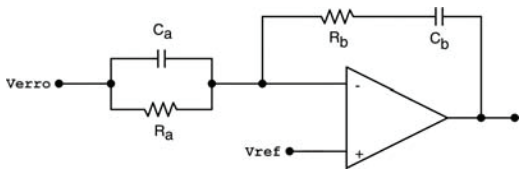

Fig. 12 Inverter controller.

The zeros of the controller match with the poles of the system, and an additional pole added at the origin establishes null error in the steady state. The inverter controller TF is given by (40).

$$C_{fb}(s) = K_{vfb} \cdot \frac{(s + \omega_{ofb}) \cdot (s + \omega_{ofb})}{s} \tag{40}$$

Establishing the crossing frequency as 8kHz, the controller gain K_{vfb} is given by (41).

$$K_{vfb} = 37 \times 10^3 \tag{41}$$

By choosing R_a=470kΩ, the controller components can be obtained from expressions (42) to (44).

$$C_a = \frac{1}{\omega_{ofb} \cdot R_a} \rightarrow C_a = 110pF \tag{42}$$

$$C_b = \frac{1}{K_v \cdot R_a} \rightarrow C_b = 22nF \tag{43}$$

$$R_b = \frac{1}{\omega_{ofb} \cdot C_b} \rightarrow R_b = 2.2k\Omega \tag{44}$$

Then, the Bode diagram of the open loop system with the designed controller $FTLAC_{fb}(s)$ is shown in Figure 13.

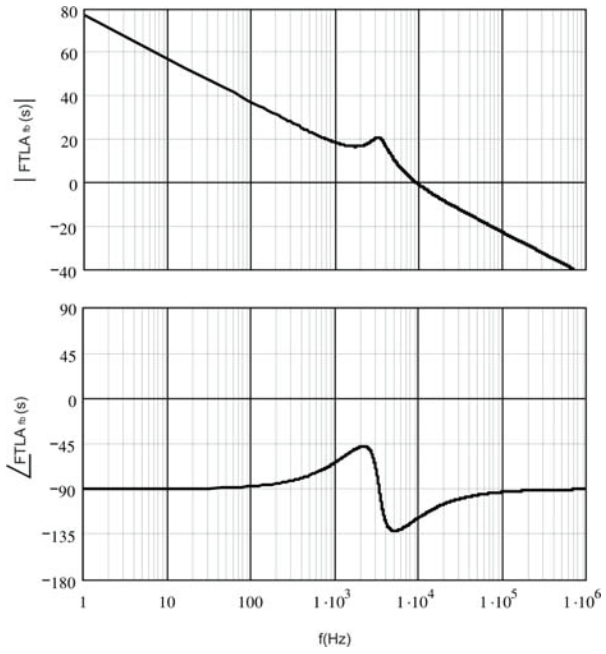

Fig. 13 Bode diagram of FTLACfb(s).

Figure 14 shows the block diagram of the dc-ac-dc stage control.

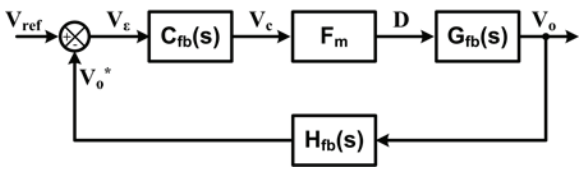

Fig. 14 Block diagram of the inverter control.

IV. EXPERIMENTAL RESULTS

Some experimental results are presented in this section. In Figure 15 one can see a low input current ripple through inductor L_1 and low voltage ripple across capacitor C_1.

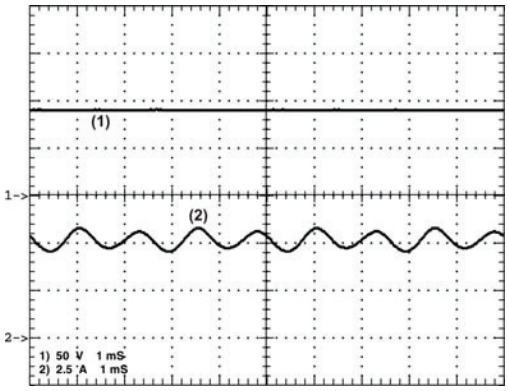

Fig. 15 Voltage ripple across the filter capacitor C_1 (1 – 50V/div) and current ripple across the filter inductor L_1 (2 – 2.5A/div).

Figure 16 shows the voltage and the current across the switches of the push-pull stage. The voltage across the switches of the push-pull stage does not contain considerable voltage peaks and stresses. The current waveform presents some oscillation due to the reverse recovery of the output diodes, but it is considered acceptable.

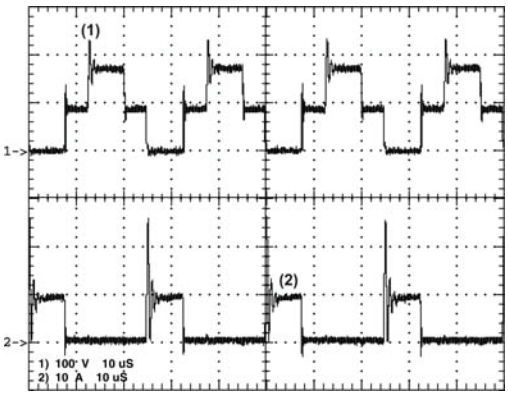

Fig. 16 Voltage across the switch in the push-pull (1 – 100V/div – 10us) and current through the primary winding of push-pull transformer (2 – 10A/div – 10us).

The Figure 17 shows the input current drained by the inverter for full linear load.

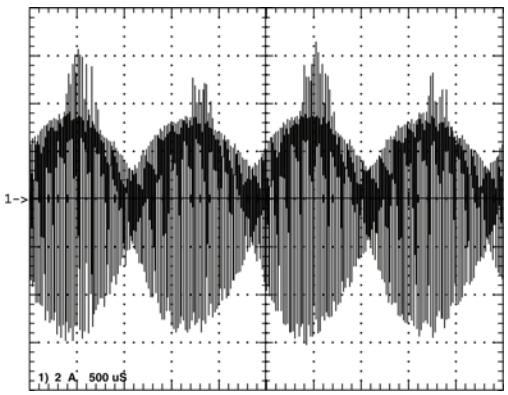

Fig. 17 Input current waveform of the inverter (2A/div – 500us).

Comparing Figure 17 with the Figure 15, it can be seen that the low frequency ripple is attenuated in L_1 current, due to the voltage loop and the filter formed by L_2 and C_2. Figure 18 shows the inverter output voltage and also the current through output inductor L_3, both for full linear load.

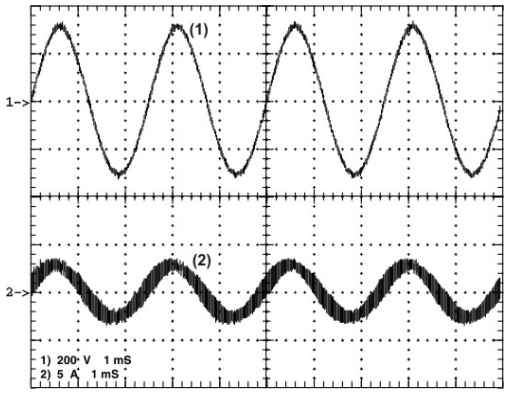

Fig. 18 Output voltage (1 – 200V/div – 1ms) and current through the filter inductor (2 – 5A/div – 1ms).

In Figure 19 one can see the harmonic spectrum of the output voltage for full linear load and the total harmonic distortion (THD) is about 2.5%.

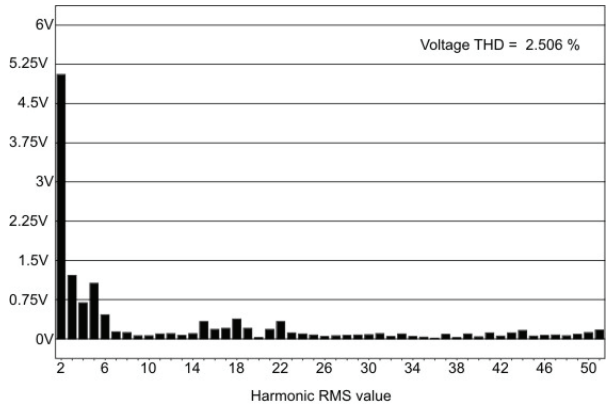

Fig. 19 Harmonic spectrum and THD of the output voltage for full linear load.

Figure 20 shows the output voltage and current through the filter inductor L_3 for a load step of the 10% for 100% of the rated load. It can be seen an optimum load step response.

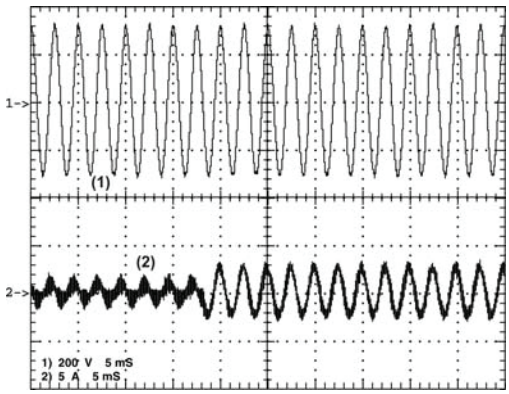

Fig. 20 Output voltage (1 – 200V/div – 5ms) and current through the filter inductor L_3 (2 – 5A/div – 5ms) for a load step of the 10% to 100% of the rated power.

Figure 21 shows the output voltage and load current for a nonlinear load.

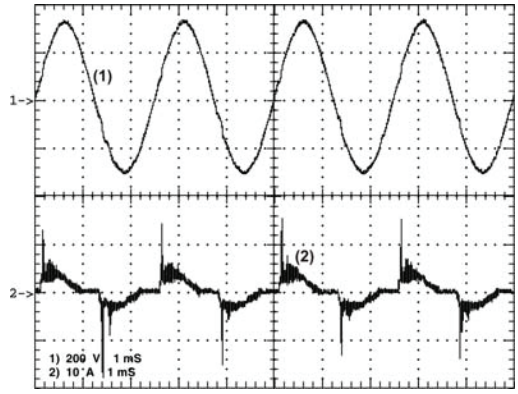

Fig. 21 Output voltage (1 – 200V/div – 1ms) and load current (2 – 10A/div – 1ms) for nonlinear load.

The harmonic spectrum and THD of the output voltage for non-linear load is shown in Figure 22. The total harmonic distortion is about 3%.

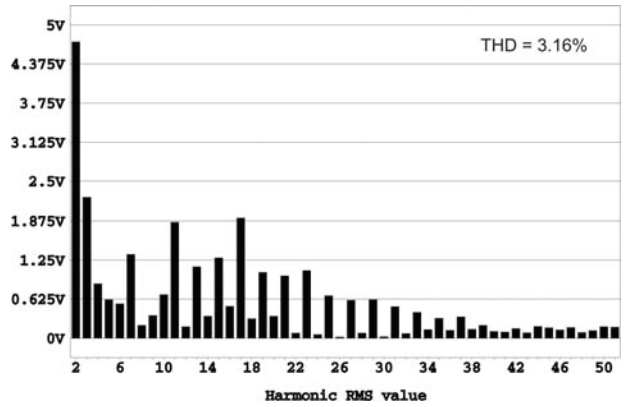

Fig. 22 Harmonic spectrum and THD of the output voltage for non-linear load.

In Figure 23 one can see the obtained global efficiency curve. The efficiency is greater than the specified.

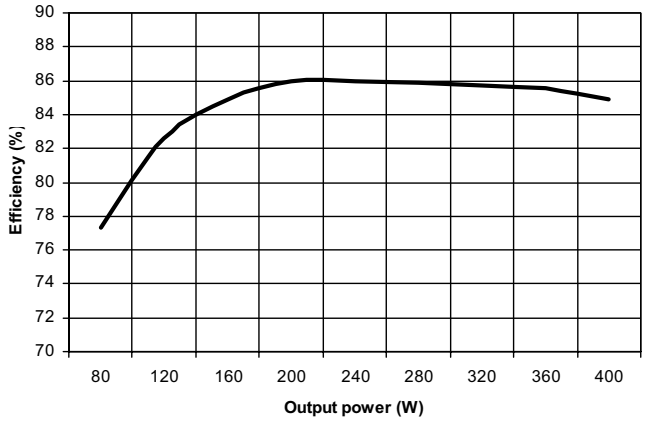

Fig. 23 Global efficiency curve.

In Figure 24 one can see the commercial prototype developed.

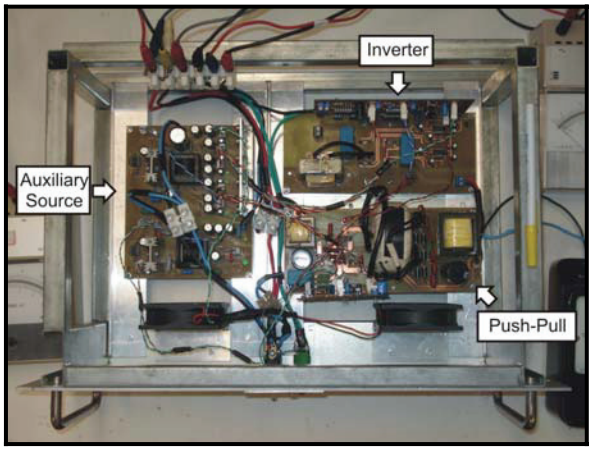

Fig. 24 Prototype picture.

V. CONCLUSION

This paper has presented a topology feasible for dc voltage sourced systems, where small input current ripple is necessary and high input voltage range exists. The low frequency component of the current injected by the inverter is attenuated by the LC output filter of the push-pull converter and by the design of the respective voltage loop controller.

The work has been supported by experimental results showing the low input current ripple, low output voltage THD and high efficiency. This equipment is currently operating in the trains of the FEPASA (Ferrovia Paulista S.A., Brazil).

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