Application of a Generalized Current Multilevel Cell to Current-Source Inverters

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***Abstract*— In this paper, a new cell which lends itself as a generic current multilevel one is applied to current-source inverters with output current harmonics minimization and without the use of high-frequency modulation. In this cell, inductors acting as current sources ensure equal current division among switches. DC current balance in the inductors is achieved, also, without closed-loop control. It is also shown that, while, for the five-level structure it is easy to find a proper control strategy, for higher levels, it is necessary to use numerical simulation programs to find out a proper switching strategy. Simulation and experimental results are included to show the performance of the new cell for high-power applications.**

***Index Terms*—Current-source inverters, multilevel converters, power electronics.**

I. Introduction

THE conventional association of semiconductor switches in series or in parallel became a common practice in the power electronics field and constitutes, even nowadays, an object of several scientific papers [1], [2]. These procedures give feasibility to high-voltage or high-current applications for which no single actual switch is able to operate. However, depending on the application and on the nature of the adopted semiconductor device, a number of requirements must be observed in order to ensure a reasonable reliability in using those technologies. An alternative to the simple association of switches is the association of converters. This technique can provide not only high-power applications, but, also, a reduction of the harmonics content. Under this concept, it is possible to associate current-source inverters (CSI's) in series [3] or in parallel [4]. Similarly, one can associate voltage-source inverters in series [5] or in parallel [6]. Another approach in the study of high-power converters changes the concept of converter association into a more general principle, by making the association of pulsewidth modulation (PWM) cells [7]. This concept has generated the multilevel converter designation and has been extensively used to reduce the harmonic distortion of a converter, as well as to provide high-voltage distribution among the employed cells [8]. Some generalized approaches for multilevel structures have also been proposed in the last decade [9], [10]. An alternative to increase the power capability of these converters, by paralleling the PWM cells, has also been proposed [11]. It seems that, until now, the multilevel concept has only been used for voltage-source converters, providing a suitable way to divide the total input voltage among a number of employed PWM cells and, also, allowing voltage harmonics reduction.

A recently introduced generic current multilevel cell [12] allows the possibility of implementation of multilevel CSI's. The multilevel CSI opens the possibility of operation with high power levels, as well as elimination of harmonics generated by the converter. The higher the level, the lower the harmonic content at the output current. An infinite number of levels ensures zero harmonic distortion at the output current waveform.

Proposed in this paper is a multilevel CSI structure, its generalization for any number of levels, the mathematical approach, and switching strategies. It is also shown that, with appropriate switching strategy for the generalized structure, current balance among the switches of the cell and an output current harmonic elimination can be reached without the use of high-frequency modulation or closed-loop control. Structures capable of up to nine levels at the output current are analyzed by simulation, and experimental results of a five-level structure are presented.

II. The Multilevel CSI Cell

The generic current multilevel cell introduced in [12] is reshaped, leading to the generic multlevel CSI, as shown in Fig. 1. Between points T_1 and T_2, there is a voltage source (or a capacitive branch) and between points C_1 and C_2 a current source (or an inductive loop).

Also, the PWM switches [12] have been adapted to a current source input, acting as a voltage bidirectional/current unidirectional switch. Any of two switches connected to the same point of a sharing inductor are complementary ones. The cell employs k PWM switches that are connected by $k-1$ inductors, which provide the current multilevel feature. It should be noted that $k=(n-1)$ and n is the number of levels of the inverter.

The generic current multilevel cell shown in Fig. 1 can be adapted to form inverters of any level, as shown in Fig. 2 for the five-level inverter.

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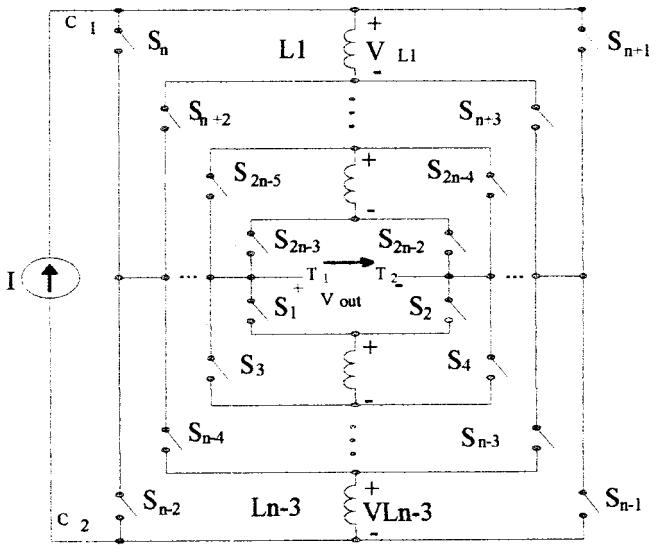


Fig. 1. The generic n-level CSI structure.

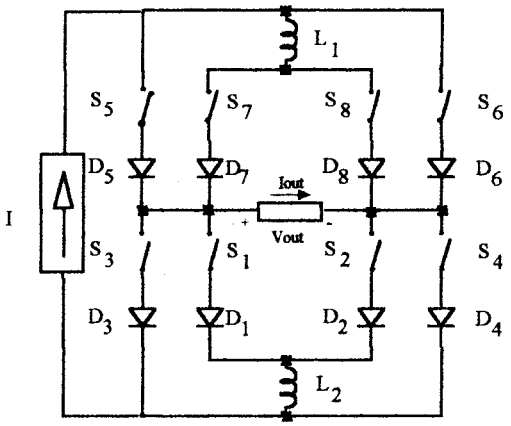


Fig. 2. The five-level CSI.

This five-level structure is made up of four pairs of parallel complementary (PWM) switches (S_5S_6, S_7S_8, S_1S_2, and S_3S_4).

From Fig. 2, one can conclude that, in order to have current equally distributed among the branches, all the switches should operste with the same duty cycle and should have the same on resistance. If they switch on and off at the same time, the switches represented by their internal on resistance "r" could be associated as a current divider and L_1 and L_2 lossless inductors carrying $I/2$.

However, to provide stepped waveform and, consequently, harmonic reduction in the load current, one of the switches of the cell must be on while the other one is off. This situation causes an alteration in the resistance balance in the proper cell, since the load branch Z_L is going to be present in one of the paths. Suppose S_5 is on and S_7 is off. Because of the complementary operation of the switches, S_8 is on and S_6 is off. One possible branch for the current I to flow is through

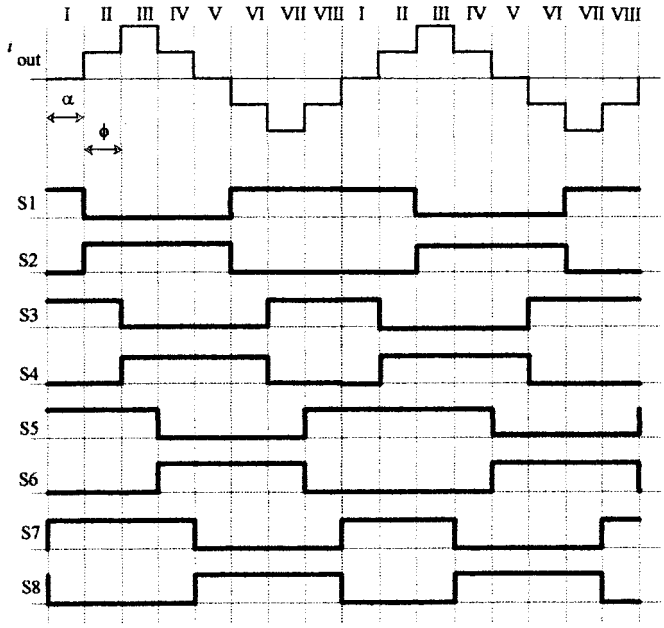


Fig. 3. Symmetric switching strategy.

the series association of L_1, S_8 and the load impedance at the output terminals T_1T_2, in parallel with S_5. In steady state, the current is going to be larger through S_5 than through S_8 if the imbalance situation described above is not compensated. For a multilevel CSI, the choice of a switching strategy that promotes the intermediate levels of the output current, even switch current distribution, power control, and harmonic minimization is, by no means, an easy task. A switching sequence is called a "symmetric strategy" if all the switches conduct precisely with a pulsewidth of 50% . If this does not happen, the strategy is called an "asymmetric strategy."

III. Symmetric Switching Strategy for Five-Level CSI

In this strategy, the switches operate with a duty cycle of 50%, as shown in Fig. 3. A similar procedure has been proposed in the structure in [4], and discussed in [13]. In Fig. 3, the parameters α and ϕ are angles associated to the time of zero and intermediate level ($+I/2$ or $-I/2$) of the output current, respectively. Note that the multilevel operation of the structure only happens for ϕ not equal to zero. It is easy to conclude that these angles are independent, and they can be chosen arbitrarily, as long as they make possible the five levels at the output current and assure zero average voltage across the sharing inductors.

The analysis of the first eight intervals of Fig. 3 shows that inductor current balance cannot be reached for one period of the output current, as analyzed in Fig. 4 for some selected intervals.

From the circuits of Fig. 4, one can conclude that the load impedance, when present in one of the branches of the cell, is always in series with the sharing inductance. This makes, in steady state, the inductance current smaller than the one of that in the other branch. To overcome this

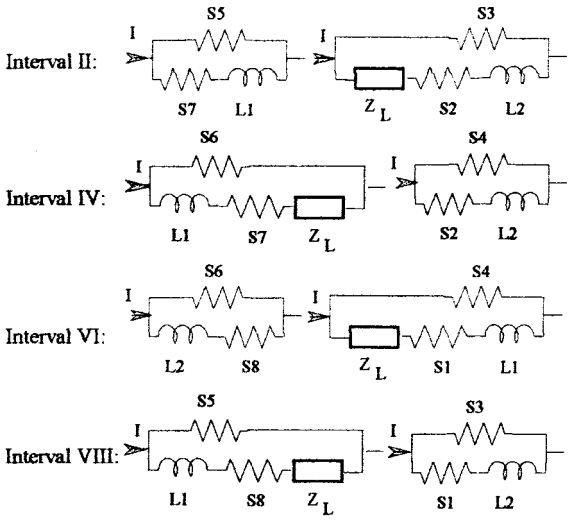


Fig. 4. Intervals in which the load impedance is part of the cell.

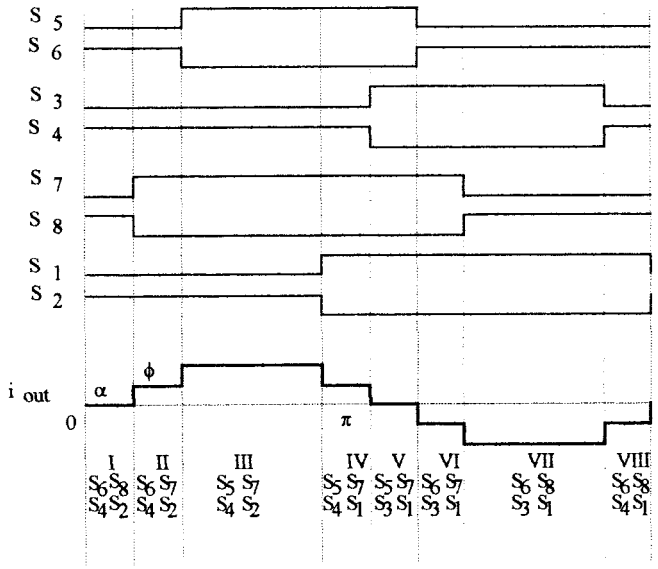


Fig. 5. Asymmetric switching strategy for output current harmonic reduction.

imbalance, a switching sequence can be chosen such that the load impedance, during the intermediate levels, is in the branch with no sharing inductance. Consider Interval II; the two paths are made of S_5S_7 and S_3S_2. The same output current could be obtained with the switches S_5S_7 and S_4S_1, and so on for the other intervals. The two switching sequences are used as shown in Fig. 3. Assuming negligible ripple, one can consider $I_{L1} = I_{L2}$. For α and ϕ of Fig. 3, the first period of the output current was provided by the following sequence: $S_5S_7S_1S_3, S_5S_7S_2S_3, S_5S_7S_2S_4$, $S_6S_3S_2S_4, S_6S_8S_1S_4, S_6S_8S_1S_3$, and $S_5S_8S_1S_3$. The same output current waveform could be obtained with the following sequence: $S_5S_7S_1S_3, S_5S_7S_1S_4, S_5S_7S_2S_4$, $S_5S_8S_2S_4, S_6S_8S_2S_4, S_6S_8S_2S_3, S_6S_8S_1S_3$, and $S_6S_7S_1S_3$.

Any of these sequences alone cannot produce a current balance in the cell. However, when one is used after the other, consecutively, as shown in Fig. 3, the result is an equilibrium in the steady-state current of the cell. Of course, the ripple in the inductors current must be small, and it is going to depend on the values of L, α, and ϕ.

IV. Asymmetric Switching Strategy

Although the symmetric strategy has the advantage of working with 50% duty cycle for any output power or harmonic spectrum, it contributes to the increase of the current ripple in the sharing reactors and, as a consequence, a higher current imbalance in the switches of the cell. This happens because it needs two periods of the output current, as shown in Fig. 3, to make the average sharing inductor voltage equal to zero. The current ripple is given by

$$\Delta I = \frac{V_{\text{out}}}{L} \cdot \Delta t \tag{1}$$

where Δt is the interval during which a balance inductor$L = L_1 = L_2$, and V_{OUT} is the output voltage (here assumed constant during this interval). By using the asymmetric switching strategy shown in Fig. 5 for $\alpha = 30°$ and $phi = 30°$, the current ripple in the sharing reactors is reduced by half, because it makes the average voltage of the inductors equal to zero for one period of the output current. The only inconvenience of this strategy is the asymmetric operation of the switches. However, for low-order harmonic elimination, the difference in the switch duty cycles is no more than 15%, when compared with the 50% duty cycle of the symmetric one. To see how this strategy works, it is necessary to analyze two intervals, II and VI of the output current in Fig. 5.

In interval II, the switches in operation are S_4S_2 and S_6S_7. The load impedance is in series with inductor L_1 and S_7. This would lead, in steady state, to an inductor current smaller than $I/2$. However, in interval VI, the switches in operation are S_3S_1 and S_6S_7, and the load impedance is, now, in series with switch S_6 only. This increases the inductor steady-state current to a value higher than $I/2$. As long as the time duration of interval II is the same as the duration of interval VI, the average current in the inductor is $I/2$. The same analysis can be made for the intervals IV and VIII, and the conclusion is that the average branch impedances are the same for one period of the output voltage.

V. Five-Level CSI Simulation Results

The performance of the five-level structure, driven by both strategies and for $\alpha = 30°$ and $\phi = 30°$, is shown in the next figures with the following parameters:

$$L_1 = L_2 = 45 \text{ mH}, \quad r_{\text{on}} = 0.1\ \Omega, \quad r_{\text{off}} = 10^6\ \Omega,$$
$$R_L = 6.3\ \Omega, \quad C_L = 100\ \mu\text{F}, \quad \text{and} \quad I = 18 \text{ A}.$$

Figs. 5 and 6 show the simulation results for the above set of parameters.

Fig. 6 shows the waveforms for the balance inductor currents and the load voltage and current at the output of the structure. Fig. 6(a) and (b) shows that the ripple currents in the sharing inductors are different. This is caused by different values of instantaneous output voltage applied to each inductor. For $\alpha = 30°$ and $\phi = 30°$, the structure

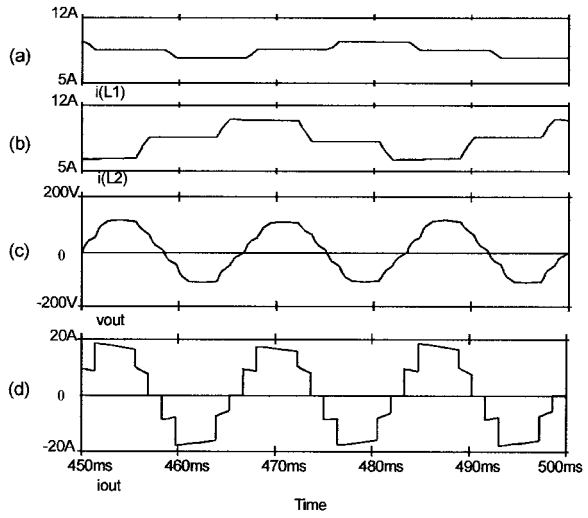


Fig. 6. Waveforms for the symmetric switching strategy. (a) Current in inductance L_1. (b) Current in inductance L_2. (c) Load voltage. (d) Output current.

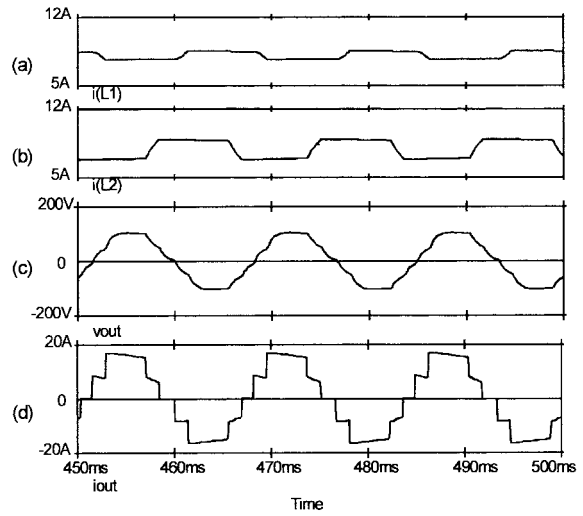


Fig. 7. Simulation results for the asymmetric strategy. (a) Current in L_1. (b) Current in L_2. (c) Load voltage. (d) Output current.

presented a good low-order harmonics minimization. The harmonic distortion factor is 12.1%. A smaller index can be computed for the filtered output voltage, 7.4%.

The behavior of the structure driven by the asymmetric switching strategy is seen in Fig. 7. One can note the smaller ripple current in the sharing inductors, when compared to the symmetric strategy in Fig. 3. That is important for the current balance in the switches of the cell. The ripple for the asymmetric strategy is half of that for the symmetric one, the simulation results show. The same parameters for symmetric and asymmetric strategies have been considered. The harmonic spectrum of the output current is similar for both strategies. The output voltage harmonic distortion is 6.1%.

VI. Output Current Control

The output current waveform is independent of the switching strategy. So, the output current control can be realized, whether for magnitude or harmonic control, by the angles α and ϕ, as defined. The waveform of the load current presents a half-wave symmetry (the sine terms are zero). It is supposed also that there is quarter-cycle symmetry. This ensures the elimination of the even harmonics. That supposition is necessary in order to ensure the same average sharing inductors current.

In this way, the harmonic coefficients of the output current are

$$A_h = \frac{2}{h\cdot\pi}\cdot\sin\left(\frac{h\cdot\pi}{2}\right)\cdot\left[\cos\left(\frac{h\cdot\alpha}{2}\right)+\cos\left(\frac{h\cdot\alpha}{2}+h\cdot\phi\right)\right] \tag{2}$$

where $h = 1,3,5,7,\cdots$.

Appropriate values for α and ϕ could be determined by the above equation in such a way that minimize the total harmonic distortion (THD) of the output current

$$\mathrm{THD}_{\%} = 100\sqrt{\frac{i_{0\mathrm{RMS}}^2}{i_{1\mathrm{RMS}}^2}-1} \tag{3}$$

where THD is given in percent, and $i_{0\mathrm{RMS}}$ and i_{RMS} are, respectively, the rms values of the output current and its fundamental component

$$i_{0\mathrm{RMS}} = \frac{\sqrt{2}}{2}I\frac{\sqrt{2\pi-(2\alpha+3\phi)}}{\pi}. \tag{4}$$

From (4), it is clear that

$$2\alpha+3\phi<2\pi. \tag{5}$$

$I_{0\mathrm{RMS}}$ in the equations above presents two degrees of liberty for different values of α and ϕ. So, one of them could be used to control the power supplied to the load and the other one to minimize the THD or to reduce some harmonic at the output current. It is clear that the output power could be controlled by changing the dc current at the CSI input. This could be done by a chopper or another converter, depending on the current source employed. This is a more comfortable situation, leaving α and ϕ to control the THD of the output current.

VII. Laboratory Prototype

To validate the use of the cell and to check out the simulation results, a laboratory prototype has been designed and constructed, as represented in Fig. 8. It has to be pointed out that, due to the low-frequency operation of the structure (60 Hz) and the nonsimultaneous operation of the switches, a sharing inductance with a value of 45 mH was necessary. The inductor was made with silicon steel, and its wiring resistance measured 0.3 Ω. In order to ensure a good current distribution, the balance inductor resistance must have a value much smaller than the on resistance of the switches.

In the experimental setup, insulated gate bipolar transistors (IGBT's) were used as active switches. It is interesting to note, however, that it would be a smart choice to use gate turn-off thyristors (GTO's) instead of IGBT's, since no diodes would

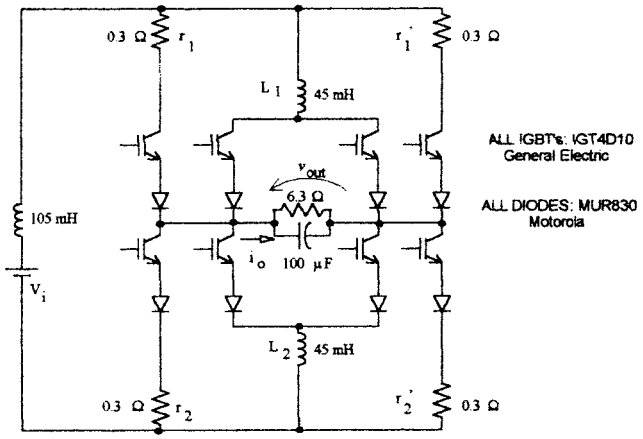


Fig. 8. Power circuit of the experimental setup.

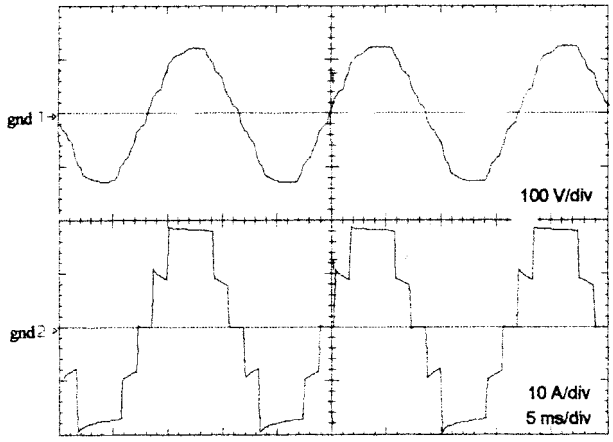
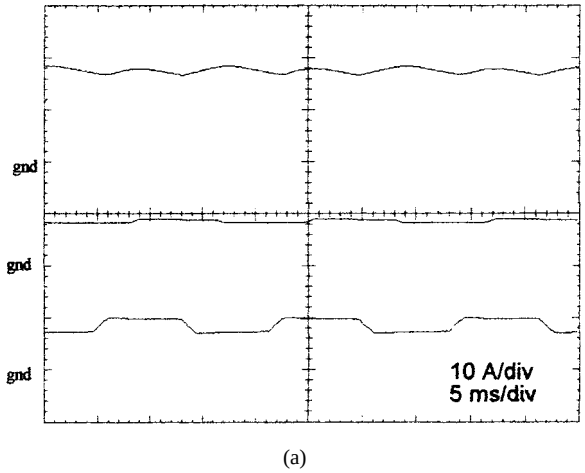
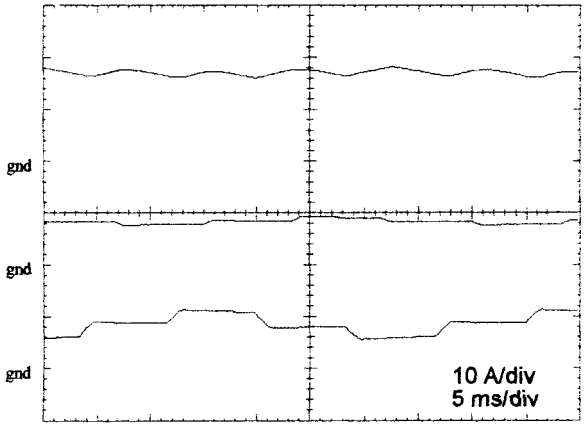


Fig. 9. Output voltage (top trace) and current.



(a)



(b)

Fig. 10. Input current (top trace), I_{L1} (middle trace), and I_{L2} (bottom trace). (a) Asymmetric strategy. (b) Symmetric strategy.

be necessary. Unfortunately, at the laboratory implementation time, this choice could not be made.

The employed IGBT's have an on resistance of 0.12 Ω, therefore, it is smaller than that of the balance inductor. This is the reason for the inclusion of the small resistors, r_1 and r_2, as shown in Fig. 8. It can be proved that this solution provides the required equilibrium of current at all branches [14]. Of course, these resistors will cause a decrease of the converter efficiency. For the adopted set of parameters, this reduction was about 4%, which could be smaller if a better technique had been used to implement the balance inductors. In the case of high current, a larger current ripple would be accepted (consequently, smaller inductors for the same output voltage). In this situation, the compensation resistor would be responsible for smaller losses. It should be mentioned that these resistances are also presented in the dual inverter structure [4], as the parasitic element of the additional inductors, which are not necessary in the five-level structure used here.

Both switching strategies were stored in electrically programmable read-only memory (EPROM), where a bit enables one or other strategy at the data bus. Each bit of the data bus is a 60-Hz signal for the eight controllable switches. Finally, the gate signals are isolated and steeped up to 13 V by a pulse transformer isolated circuit.

The measured output power for the structure in Fig. 8 was 1.2 kW. The input current source was obtained from a dc voltage source V_i in series with a 105-mH inductor.

TABLE I
POSSIBLE COMBINATIONS FOR THE FIVE-LEVEL STRUCTURE

Combination	S_1S_3	S_5S_7	I_o	V_{L1}	V_{L2}
0	00	00	0	0	0
1	00	01	1	−1	0
2	00	10	1	+1	0
3	00	11	2	0	0
4	01	00	−1	0	−1
5	01	01	0	−1	−1
6	01	10	0	+1	−1
7	01	11	1	0	−1
8	10	00	−1	0	+1
9	10	01	0	−1	+1
10	10	10	0	+1	+1
11	10	11	1	0	+1
12	11	00	−2	0	0
13	11	01	−1	−1	0
14	11	10	−1	+1	0
15	11	11	0	0	0

TABLE II
COMBINATIONS AND SIMPLE SEQUENCIES FOR ONE PERIOD ONLY

n	Load Current Levels					N_C	N_S
	0	±1	±2	±3	±4		
3	2	1				4	4
5	6	4	1			16	9216
7	20	15	6	1		64	$2{,}62\text{x}10^4$
9	70	56	28	8	1	256	$1{,}21\text{x}10^{20}$

TABLE III
EXAMPLES OF REAL SEQUENCIES FOR $n = 7$ AND $n = 9$

n	z	Real Sequencies
7	3	56 57 61 63 47 39 7 5 1 0 32 40 56 60 62 63 31 15 7 6 4 0 8 24 56 58 59 63 55 23 7 3 2 0 16 48
9	4	240 248 252 254 255 239 207 143 15 31 63 127 255 247 243 241 240 244 252 253 255 223 207 79 15 47 63 191 255 251 243 242 240 176 48 32 0 2 3 11 15 13 12 4 0 64 192 208 240 112 48 16 0 1 3 7 15 14 12 8 0 128 192 224

Fig. 9 shows the output voltage and current of the five-level inverter. The load is made of a parallel *RC* combination, being $R = 6.3\ \Omega$ and $C = 100\ \mu$F. The harmonic analysis yields a 5.5% and 15.5% THD for the output voltage and current, respectively. The current ripple in the sharing reactors is shown in Fig. 10 for both strategies.

VIII. SWITCHING STRATEGY ALGORITHM

The switching sequences for the five-level structure can be easily determined by inspection, as was done in Sections III and IV. On the other hand, for the seven-level structure and above, a greater difficulty is noticed due to the high number of possible combinations of the switches. In such cases, it is necessary to use a numeric algorithm to find the switching sequences.

The first step consists in determining, for every combination, the output current level and the voltages on the inductors. The results for the five-level structure seen in Fig. 3 is presented in Table I.

The setup of that combination table, for a five-level structure (which can be extended for n-level) can be done by the following algorithm.

1) The number of combinations of an n-level structure is equal to $Nc = 2^{(n-1)}$. The column named "combination" is formed by the 16 possible combinations of the five-level structure. This column associates every combination with a number of which binary representation informs the state of the odd switches.
2) The next two columns present the states of the odd switches of the structure. The number of switches of the structure is equal to $2 \cdot (n-1)$, and the number of odd switches is equal to $(n-1)$. The combination number is represented in binary form and divided into two parts (most and least significant parts), which are shown in the two columns that describe the state of the switches.
3) The column that indicates the level of the output current (I_{out}) is equal to the sum of the quantity of 1's of the least significant half (represented in binary form) minus the quantity of 1's of the most significant half. In Table I, the value of I_{out} is given by the summation of the quantity of 1's of the column S_5S_7 minus the summation of the quantity of 1's of the column S_1S_3. This procedure could be easily verified observing the inverter structure. The switches in the structure have been numbered in such a way to permit the assembling of the combination tables according to this algorithm.
4) The last columns represent the voltages on the sharing inductors. Observing the n-level structure in Fig. 1, it can be concluded that the voltage on each inductor depends only on the state of two odd switches. The instantaneous voltage on an inductor either is zero (when the inductor is shorted by two switches) or equal to the load voltage with polarity, depending on the state of the switches. The voltage on an inductor can be determined as shown in the following example.

Consider the inductor L_1 of the five-level inverter shown in Fig. 3. The voltage across L_1 depends on the state of S_7 and S_5 and the load voltage V_{out}. If both S_7 and S_5 are on or off, L_1 is short circuited and $V_{L1} = 0$. If the states S_5 and S_7 are 01 or 10, then $V_{L1} = V_{\text{out}}$ or $V_{L1} = -V_{\text{out}}$, respectively.

Once the combination table is obtained, the help of a digital algorithm is necessary to solve the problem of the current imbalance, that is, to find viable switching sequencies. For an organized treatment of the matter, some terms are defined below.

1) *Combination* is a set of possible conducting switches during a dertemined interval of time.
2) *Simple sequence* is an organized set of combinations that leads to the desired waveform, assuming the sharing inductors are independent current sources.
3) *Sequence of a z size* is a sequence related with z periods of the desired output current.

4) *Minimum frequency sequence* is an organized sequence with successive combinations which differ by one bit only (the state of an odd switch).
5) *Real sequence* is a minimum frequency sequence that guarantees zero average voltage in the sharing inductors within a minimum number of cycles.

For the determination of the real sequences, the following should be considered.

1) The frequency of operation of the switches should be the same as the converter fundamental output frequency.
2) The switches should conduct the same average current. One of the objectives of the multilevel structure is the even current distribution among the switches of a cell.
3) Limitation of the peak current magnitude in a switch should be considered. A low ratio average value/rms value has to be avoided.
4) Reduction in the output harmonic content should also be considered. This is obtained by selecting proper width of the output current several levels.
5) The structure operation should be independent of the load. The multilevel inverter output current waveform should be independent of the structure output voltage.
6) The steady-state average voltage on each inductor of the structure must be zero. Otherwise, no current balance in the switches of the cell is obtained [4].

Table I shows that, for the five-level converter $(n = 5)$, there are 16 possible combinations. In general,

$$N_c = 2^{(n-1)}. \tag{6}$$

For $n = 7$, there are 64 combinations, for $n = 9$ there are 256 combinations, and so on.

It should be pointed out that any switching sequence has to contain the combinations 3 and 12 for maximum and minimum levels $(\pm I)$. There are six options of level zero and four of intermediate levels $(\pm I/2)$. It is possible to conclude that there are two levels of 0, $+I/2$ and $-I/2$. So, the number of possible simple sequences of one period N_s is

$$N_s = N_0^2 \cdot N_1^4 \cdot N_2^4 \cdots N_{n-1}^4 \cdot N_n^0.$$

Where N_0 is the number of combinations of zero current at the load, N_1 is the number of combinations for the first intermediate level, N_2 for the second, and so on.

Table II shows the basic information for three-, five-, seven-, and nine-level converters.

It is clear that the number of simple sequences is too high and does not reflect practical possibilities that exist only in the real sequences. The developed algorithm sees all the possibilities and gets the minimum frequency sequences and then the real sequences. For a converter with $n \geq 5$, there are no real sequences of one period only. So, for $n = 5$, the sequences must have two periods of the output current, for $n = 7$ three periods, and for $n = 9$ four periods. Using the algorithm (developed in C language) for determining the sequences, real sequences for $n = 7$ and $n = 9$ were determined, as shown in Table III.

IX. Conclusion

The application of a new current multilevel cell to a CSI structure has been presented. The concept of current multilevel converters has been introduced here. The main advantages to the use of the new cell are the possibility of generalization to n level in the output current and the need of less sharing reactors than other known structures [4], [13]. With a proper switching strategy, it is possible to reduce the size of the sharing reactors and eliminate some harmonics of the output current without the use of high-frequency modulation. All of these advantages suggest the use of the structure in high-power applications.

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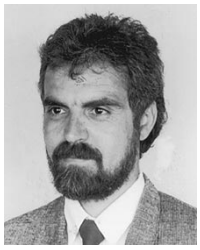

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