Analysis, Design, and Experimentation of a Double Forward Converter With Soft Switching Characteristics for All Switches

Demercil de Souza Oliveira, Jr., Carlos Elmano de Alencar e Silva, René Pastor Torrico-Bascopé, Fernando Lessa Tofoli, Carlos Augusto Bissochi, Jr., João Batista Vieira, Jr., Valdeir José Farias, and Luiz Carlos de Freitas

***Abstract*—The study of a topology resulting from the combination of two forward structures attached to a single transformer core is presented in this paper, as a dual active bridge converter is obtained. In order to reduce the switching losses and the electromagnetic interference, a soft commutation cell, which provides zero-voltage commutation of the main switches for the entire load range, is implemented. Besides, the auxiliary switches are zero-current turned on and zero-current, zero-voltage turned off. This converter reduces the voltage over the main switches to half of the input voltage, employing only four switches and an additional transformer winding when compared to the full-bridge converter. The analysis of the circuit is carried out, and experimental results obtained from a prototype are also presented to support the theoretical assumptions.**

***Index Terms*—Dual active bridge (DAB), isolated converters, soft switching.**

I. Introduction

THERE is an increasing demand for high-density power converters, whereas in most cases, the size of the magnetic components, including transformers and inductors, significantly influences the overall performance of the converters. In many applications, isolated converters are preferred in order to reduce electromagnetic interference (EMI) levels and comply with technical insurance standards. Generally, there are two dominant types of isolated topologies: 1) buck mode topologies such as forward [1], push–pull [2], half-bridge [3], and full-bridge [4]; and 2) buck–boost mode topologies such as dual flyback [5].

The conventional forward converter with resonant reset presents simple circuitry, although good reset condition over entire line and load conditions is hard to maintain. The two-switch forward converter comes as an alternative to achieve the lowest voltage stress across the switches, with the addition of an extra switch and a high-side gate driver, and 50% maximum duty ratio limitation [6], [7].

Typically at power levels higher than 500 W, the phase-shift full bridge (PSFB) dc–dc converter is preferred due to its high efficiency and low EMI [8]. However, the circulating loss in primary is high for a conventional PSFB converter especially in high input current application. Based on [9] and [10], soft-switching techniques have been proposed for pulse width modulation (PWM) full-bridge converter and can be classified into two types: one is zero-voltage switching (ZVS) [11] and the other is zero-voltage and zero-current switching (ZVZCS) [12]. In ZVZCS PWM full-bridge converters, one leg achieves ZVS and the other leg achieves ZCS [13], but there is serious voltage oscillation across the rectifier diodes caused by the reverse recovery no matter if ZVS or ZVZCS is realized for the switches [14].

The dual active bridge (DAB) dc–dc converter has been proposed in [15]. The circuit realizes ZVS of all switches while achieving synchronous rectifiers at the output side. Besides, compared to the conventional full-bridge converter, such isolated dc–dc converters have lower input current ripple, less stress on power switching components, and smaller output filter inductor [16], [17].

Though the DAB converter has some attractive features [18], the circulation energy flowing back from output to input is still quite large, which causes high conduction losses and high current ripple flowing through the output filter capacitors. The circulation energy varies with the output power, output voltage, and input voltage. Commonly, the circulation energy can reach 25% of the total output power at maximum output power.

An interesting topology was obtained from the association of two two-switch forward converters supplying two primary windings [19]. A new converter that can operate as a full-bridge structure results, as the complete hysteresis cycle of the transformer can be used. Besides, the output filter is designed for twice the switching frequency of a single forward topology, such as in the full-bridge converter. A similar topology with only two switches was introduced in [20]. However, there is no natural path for the leakage energy, what causes additional voltage stress and loss in the main switches, limiting their power capacity.

Manuscript received June 28, 2010; revised November 29, 2010; accepted December 27, 2010. Date of current version August 10, 2011. Recommended for publication by Associate Editor J. A. Cobos.

D. de Souza Oliveira, C. E. de Alencar e Silva, and R. P. Torrico-Bascopé are with the Department of Electrical Engineering, Federal University of Ceará, Fortaleza CEP 60455760, Brazil (e-mail: demercil@dee.ufc.br; elmano@ufc.br; rene@dee.ufc.br).

F. L. Tofoli is with the Department of Electrical Engineering, Federal University of São João del-Rei, São João del-Rei CEP 36307352, Brazil (e-mail: fernandolessa@ufsj.edu.br).

C. A. Bissochi, J. B. Vieira, V. J. Farias, and L. C. de Freitas are with the Department of Electrical Engineering, Federal University of Uberlândia, Uberlândia CEP 38400902, Brazil (e-mail: cabjunior@ufu.br; batista@ufu.br; farias@ufu.br; freitas@ufu.br).

Digital Object Identifier 10.1109/TPEL.2010.2104331

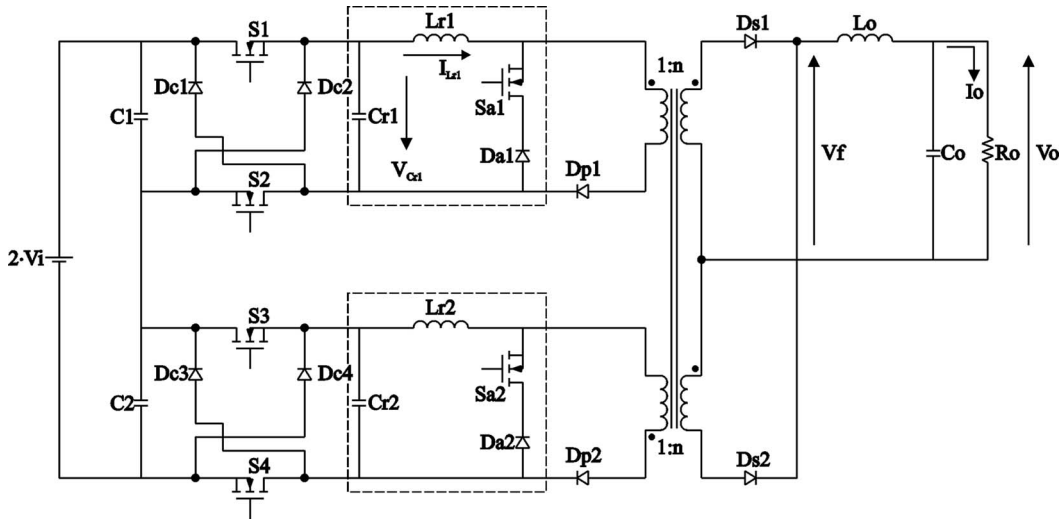


Fig. 1. Proposed converter.

In order to achieve soft commutation for all switches, some solutions have been proposed in the literature, which are described as follows. The modulation technique presented in [21], associated with the use of an additional secondary inductor, provides soft commutation for all switches. However, the load range in which soft commutation is achieved depends on the design of the resonant elements. Additionally, there is reactive energy flow through the primary side when duty cycle is small. Both factors tend to compromise the efficiency of the converter.

The use of auxiliary inductors in the achievement of ZVS commutation is proposed in [22]. Although soft commutation over the full load range is possible without using series inductors, the introduced reactive energy reduces efficiency. The use of coupled resonant inductors in [23] is an alternative to reduce the number of auxiliary components and minimize the duty cycle loss. However, the load range in which soft commutation is achieved and also the circulating current compromise the efficiency as well.

With the advent of digital signal processors (DSPs), the implementation of several control strategies to provide better dynamic and static performance than the traditional phase-shift control has become possible. The work described in [24] uses distributed power system control to decrease peak current, eliminate reactive power, increase power capability, increase system efficiency, and minimize the output capacitance in a dual-bridge bidirectional converter. However, it leads to increased cost and complexity if compared with conventional solutions such as that proposed in [25] for a bidirectional DAB converter.

Within this context, this paper proposes the use of auxiliary switches in order to achieve soft commutation. The auxiliary cell provides ZVS of the main switches during turn-on and turn-off, respectively [26], [27], for the full-load range. Additionally, the auxiliary switches achieve zero-current switching (ZCS) during turn-on and zero-current, zero-voltage switching during turn-off (ZCZVS). The use of the cell allows obtaining high switching frequency operation, high power, and high efficiency for a wide load range with reduced EMI levels.

II. Proposed Topology

Fig. 1 shows the proposed topology where the soft switching cells are represented in the dashed lines for each one of the forward converters. As it can be seen, there is one forward structure associated with each primary winding, but a single core is used. This arrangement uses the complete hysteresis cycle of the transformer such as the push–pull converter does [2], where the currents through the primary windings are unidirectional. The output filter is designed for twice the switching frequency of the main switches. This results in a converter which presents characteristics similar to the full-bridge topology.

Active snubbers can reduce the switching losses by using auxiliary switches. Unfortunately, an auxiliary switch increases the complexity of both power and control circuits. Synchronization problems between control signals of the switches during transient also complicate the control strategy. Circuit cost is increased and reliability is affected by using active snubbers.

Although two additional auxiliary switches are included in the proposed converter, cost is similar to that of the aforementioned solutions since the switches only deal with the resonant energy. The resonant inductor can be small, not only due to the resonance frequency chosen as ten times the switching frequency, but also because it is supposed to be rated only for the peak of the resonant current, although it must conduct the load current. Furthermore, soft switching is achieved for the entire load range, what is difficult to obtain when dealing with passive snubbers [28].

It must also be mentioned that the concept involving this structure, which is able to operate in current sharing mode [29], [30], can be extended to any number of converters using a single transformer core. The resulting voltage across the switches is $V_i/2a$, where V_i is the input voltage and a is the number of associated converters.

A. Operating Principle

The operation of the converter shown in Fig. 1 can be explained in six stages, according to Fig. 2. The main theoretical

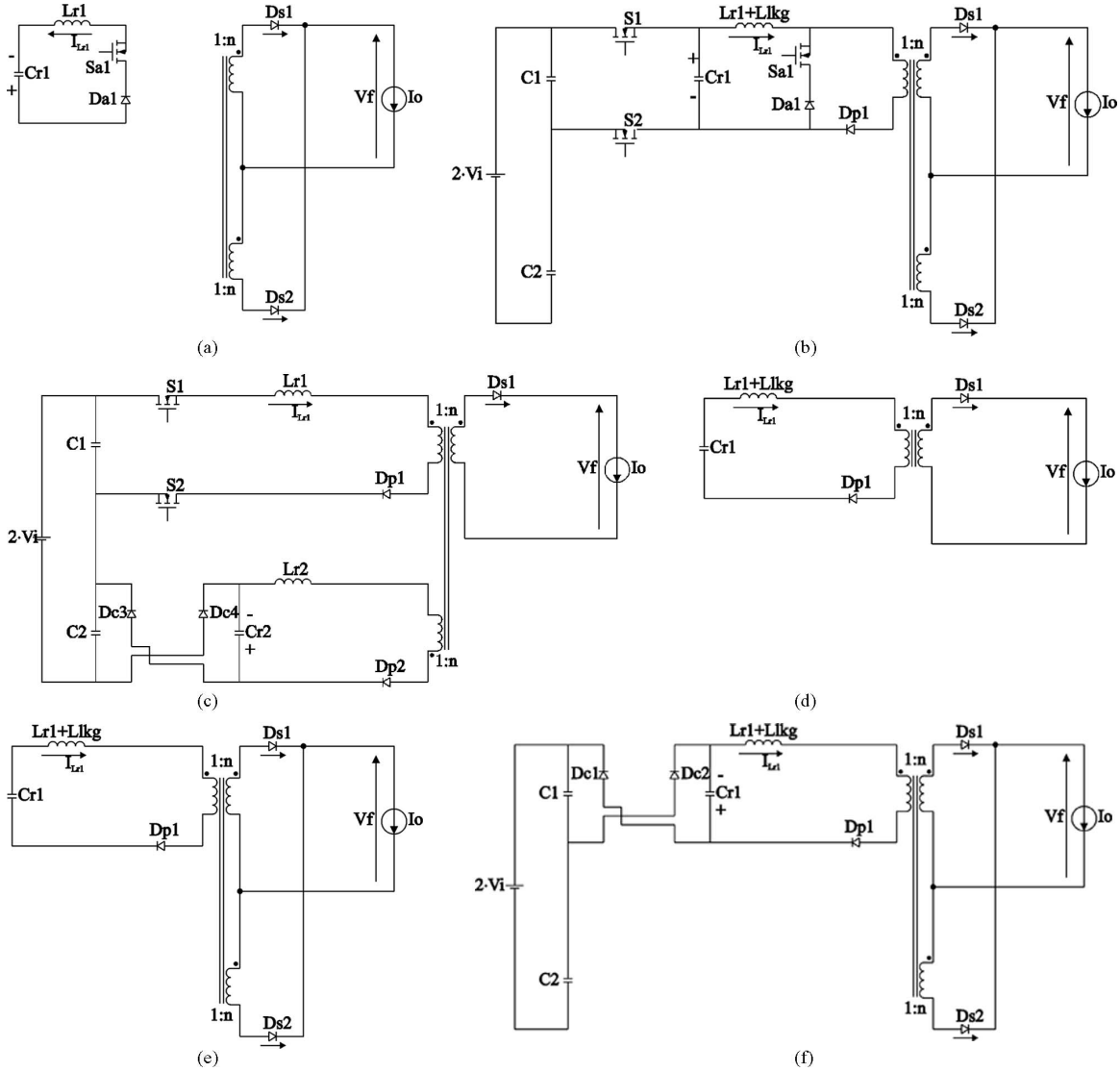


Fig. 2. Operating stages. (a) First stage. (b) Second stage. (c) Third stage. (d) Fourth stage. (e) Fifth stage. (f) Sixth stage.

waveforms are shown in Fig. 3, which characterize the behavior of the circuit during one switching period. The voltage across the primary winding and the gating signal of a given switch are represented in Fig. 3 by V_p and V_g, respectively.

It must be mentioned that the mathematical study carried out in this section considers the voltages and currents as represented in Fig. 1. In order to simplify the analysis, the following conditions are assumed:

1) all semiconductors are ideal;
2) the total input voltage is expressed as $2V_i$;
3) the output voltage V_0 and the current through output inductor L_0 are constant and ripple-free;
4) the output stage is represented by a dc current source I_0 that corresponds to the load current;
5) V_f is the voltage across the output filter;
6) the voltages across C_1 and C_2 are equal to V_i and ripple-free;
7) the transformer ratio between the primary and secondary windings is defined by n.
8) duty cycle D is defined as $D \leq 0.5$.

Besides, the following parameters are defined:

$$\alpha = \frac{I_0}{nV_i}\sqrt{\frac{L_{r1}}{C_{r1}}} \tag{1}$$

$$Z_0 = \sqrt{\frac{L_{r1}}{C_{r1}}} \tag{2}$$

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_{r1}C_{r1}}} \tag{3}$$

where

α	normalized load current (A);
I_0	load current (A);
n	turns ratio;
L_{r1}	resonant inductor of the upper cell (H);
C_{r1}	resonant capacitor of the upper cell (F);
Z_0	characteristic impedance (Ω);
ω_0	resonance frequency (rad/s).

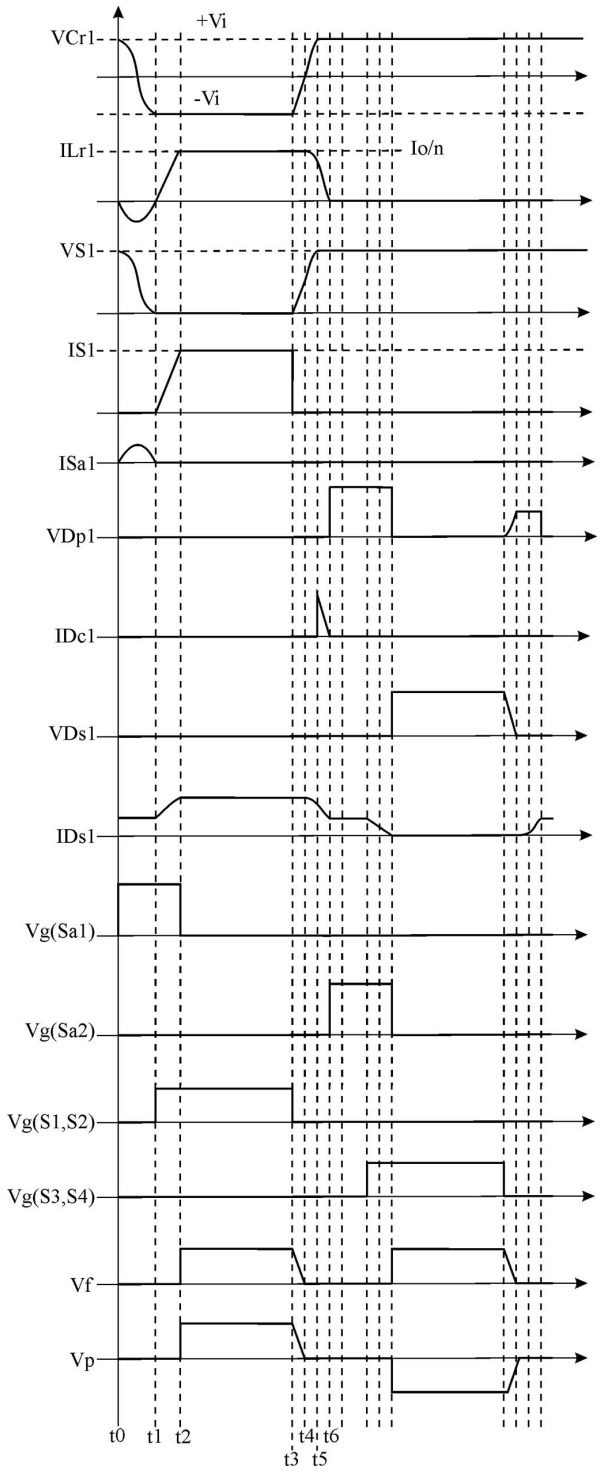


Fig. 3. Theoretical waveforms.

1) First Stage [t_0, t_1] [Fig. 2(a)]: At the beginning of the stage, both main switches are turned off and auxiliary switch S_{a1} is turned on under null current condition. Initially, the voltage across capacitor C_{r1} is $+V_i$ and the current through L_{r1} is null. Then, resonance occurs between capacitor C_{r1} and inductor L_{r1} until the voltage across C_{r1} equals $-V_i$. During this stage, the secondary diodes conduct the load current.

Analyzing Fig. 2(a), the expressions that determine the current through the resonant inductor and the voltage across the resonant capacitor can be obtained as

$$i_{Lr1}(t) = -\frac{V_i}{Z_0}\sin(\omega_0 t) \tag{4}$$

$$v_{Cr1}(t) = V_i \cdot \cos(\omega_0 t). \tag{5}$$

The interval that defines this stage is

$$\Delta t_1 = t_1 - t_0 = \frac{1}{2 \cdot f_0} \tag{6}$$

where f_0 is the resonance frequency (Hz).

2) Second Stage [t_1, t_2] [Fig. 2(b)]: When the voltage across C_{r1} equals $-V_i$, main switches S_1 and S_2 can be turned on under zero-voltage condition, and the current through L_{r1}, i.e., $i_{Lr1}(t)$ starts increasing linearly. Consequently, the currents through secondary diodes D_{s1} and D_{s2} in Fig. 2(b) are supposed to increase and decrease linearly, respectively. This stage finishes when $i_{Lr1}(t)$ equals the load current.

During the second stage, the current through L_{r1} can be expressed by

$$i_{L_{r1}}(t) = \frac{V_i}{L_{r1}} \cdot t = \frac{\omega_0 I_0}{n\alpha} \cdot t = \frac{V_i \cdot \omega_0}{Z_0} \cdot t. \tag{7}$$

The time interval Δt_2 depends on the load and is calculated by

$$\Delta t_2 = t_2 - t_1 = \frac{\alpha}{\omega_0} \cdot \frac{L_{r1} + L_{lkg}}{L_{r1}} \tag{8}$$

where L_{lkg} is the leakage inductance of the transformer.

3) Third Stage [t_2, t_3] [Fig. 2(c)]: When the current through L_{r1} equals I_0/n, energy transfer begins and auxiliary switch S_{a1} can be turned off. The load current flows through diode D_{s1}, as diode D_{s2} is blocked. Additionally, the capacitor C_{r2} is charged to $+V_i$.

From Fig. 2(c), the following expressions can be obtained:

$$i_{L_{r1}}(t) = \frac{I_0}{n} = \frac{\alpha V_i}{Z_0} \tag{9}$$

$$v_{C_{r1}}(t) = -V_i. \tag{10}$$

The time interval Δt_3 depends on the duty cycle imposed by the control circuit and is given as

$$\Delta t_3 = t_3 - t_2 = D \cdot T_s - \frac{\alpha}{\omega_0} \cdot \frac{L_{r1} + L_{lkg}}{L_{r1}} \tag{11}$$

where T_s is the switching period.

4) Fourth Stage [t_3, t_4] [Fig. 2(d)]: Main switches S_1 and S_2 are turned off at the beginning of this stage. The current through L_{r1} remains constant and equal to I_0, as capacitor C_{r1} is discharged linearly. This stage finishes when C_{r1} is completely discharged, as diode D_{s2} is forward biased and the voltage across the transformer windings remains null.

During this stage, the following expressions are valid:

$$i_{L_{r1}}(t) = \frac{\alpha V_i}{Z_0} \tag{12}$$

$$v_{C_{r1}}(t) = V_i \cdot (\alpha\omega_0 \cdot t - 1). \tag{13}$$

The time interval that corresponds to this stage is

$$\Delta t_4 = t_4 - t_3 = \frac{1}{\alpha \cdot \omega_0}. \tag{14}$$

5) Fifth Stage [t_4, t_5] [Fig. 2(e)]: This stage begins when diode D_{s2} is forward biased, keeping the voltage across the transformer windings null. Resonance between L_{r1} and C_{r1} persists while the inductor is not completely discharged or the voltage across resonant capacitor C_{r1} does not equal $+V_i$.

The expressions that describe the behavior of this stage are

$$i_{L_{r1}}(t) = \frac{\alpha V_i}{Z_0} \cdot \cos(\omega_0 t) \tag{15}$$

$$v_{C_{r1}}(t) = \alpha \cdot V_i \cdot \sin(\omega_0 t). \tag{16}$$

The time interval Δt_5 depends on the load and is given as

$$\Delta t_5 = t_5 - t_4 = \begin{cases} \dfrac{1}{4 \cdot f_0}, & \text{if} \quad \alpha < 1 \\ \dfrac{\sqrt{L_{r1} + L_{lkg}/L_{r1}}}{\omega_0} \cdot \sin^{-1}\left(\dfrac{1}{\alpha}\right), & \text{if} \quad \alpha \geq 1. \end{cases} \tag{17}$$

6) Sixth Stage [t_5, t_6] [Fig. 2(f)]: If the voltage across C_{r1} equals $+V_i$ before the current through L_{r1} becomes null (heavy load condition), the remaining current will flow through cross diodes D_{c1} and D_{c2}, as it decreases linearly until zero. If this condition is not achieved, i.e., $\alpha < 1$, this stage will not exist.

When the sixth stage finishes, a new switching cycle begins for the lower leg of the dual-bridge converter, as auxiliary switch S_{a2} is initially turned on. Later on, main switches S_3 and S_4 take part in the operation of the circuit.

The current through the resonant inductor can be obtained from

$$i_{L_{r1}}(t) = \frac{V_i}{Z_0}(\sqrt{\alpha^2 - 1} - \omega_0 t). \tag{18}$$

The time interval that describes this stage is

$$\Delta t_6 = t_6 - t_5 = \frac{L_{r1} + L_{lkg}}{L_{r1}} \cdot \frac{\sqrt{\alpha^2 - 1}}{\omega_0}. \tag{19}$$

B. Static Characteristic of the Converter

The static gain can be calculated from

$$G = \frac{V_{f(\text{avg.})}}{V_i} \tag{20}$$

where

G static gain;

$V_{f(\text{avg.})}$ average voltage across the output filter, given by (21) (V).

$$V_{f(\text{avg.})} = \frac{2}{T_s} \cdot \int_{t=0}^{t=(T_s/2)} v_f(t) \cdot dt. \tag{21}$$

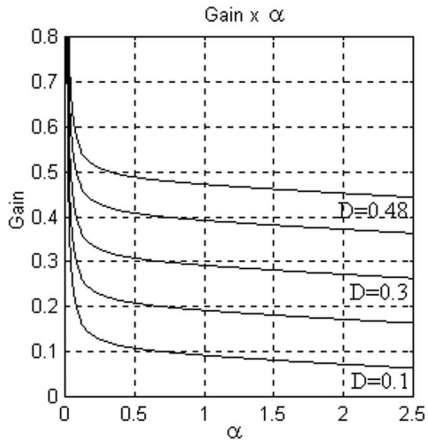


Fig. 4. Static gain.

There is energy transfer during the third stage. Then, (21) can be rearranged as

$$V_{f(\text{avg.})} = \frac{2}{T_s} \cdot \left[\int_{t=0}^{t=\Delta t_3} \frac{V_i}{n} \cdot dt + \int_{t=0}^{t=\Delta t_4} -\frac{1}{n} \cdot \left(\frac{I_0}{n \cdot C_{r1}} t - V_i\right) dt\right] \tag{22}$$

where Δt_3 and Δt_4 are the time intervals that define the third and fourth stages, respectively.

Substituting (22) into (20) gives the static gain as

$$G = \frac{1}{n}\left[D - \frac{f_s}{f_0} \cdot \left(\frac{L_{r1} + L_{lkg}}{L_{r1}} \cdot \alpha - \frac{1}{2\alpha}\right) \cdot \frac{1}{2\pi}\right]. \tag{23}$$

Considering $n = 1$, $L_{lkg} = 0$, and $f_s/f_0 = 0.1$, the static gain curves can be plotted as in Fig. 4.

Another important parameter to be determined is the maximum effective duty cycle $D_{\max}$, which is calculated from

$$D_{\max} = \sum_{i=1}^{6} \Delta t_i = \frac{T_s}{2}. \tag{24}$$

Substituting (6)–(19) into (24) gives

$$D_{\max} = \frac{1}{2} - \frac{f_s}{f_0} \cdot \left(\frac{1}{2} + \frac{1}{2\pi\alpha} + \frac{1}{\pi} \cdot \sin^{-1}\left(\frac{1}{\alpha}\right) + \frac{\alpha}{\pi\sqrt{1 + \alpha^2}}\right). \tag{25}$$

Expression (25) can be plotted as in Fig. 5, where it can be seen that $D_{\max}$ is limited by the normalized load current.

As one can see, the static gain shows clearly the output response for different load situations. However, the static characteristic is not enough to design the converter adequately. A more interesting graph that shows the maximum power transfer capability can be obtained in Fig. 6 by combining (23) and (25), as the leakage inductance is considered null.

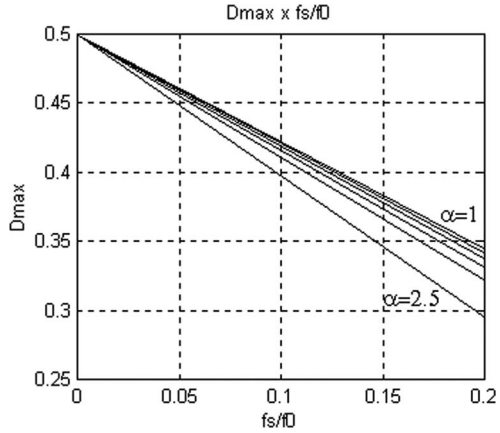


Fig. 5. Maximum effective duty cycle.

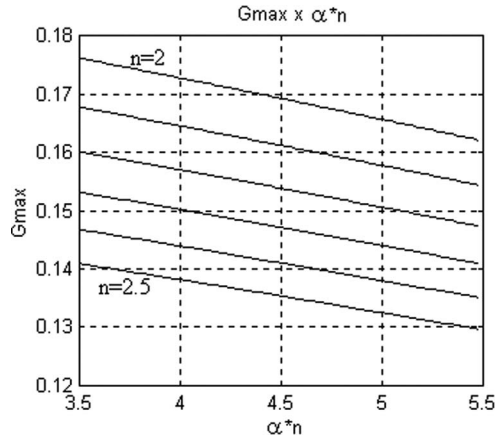


Fig. 6. Maximum static gain as a function of $\alpha \cdot n$, for $L_{lkg} = 0$.

C. Stresses Involving the Semiconductor Elements

The average and rms currents through main switches S_1, S_2, S_3, and S_4 can be obtained from (26) and (27), respectively

$$I_{S(\text{avg})} = \frac{V_i \cdot \alpha}{Z_0} D - \frac{f_s}{f_0} \frac{V_i \cdot \alpha^2}{4\pi Z_0} \tag{26}$$

$$I_{S(\text{rms})} = \frac{\alpha V_i}{Z_0} \cdot \sqrt{D - \frac{f_S}{f_0} \cdot \frac{\alpha}{3\pi}}. \tag{27}$$

The average and rms currents through auxiliary switches S_{a1} and S_{a2} can be obtained from (28) and (29), respectively

$$I_{Sa(\text{avg})} = -\frac{f_s}{f_0} \cdot \frac{V_i}{\pi Z_0} \tag{28}$$

$$I_{Sa(\text{rms})} = \frac{V_i}{2Z_0} \cdot \sqrt{\frac{f_s}{f_0}}. \tag{29}$$

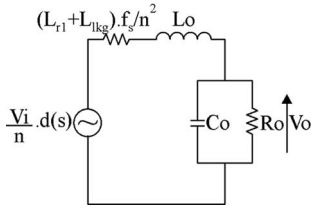


Fig. 7. Small signal model of the proposed converter.

TABLE I
COMPARISON BETWEEN THE DUAL-BRIDGE CONVERTER AND THE FULL-BRIDGE TOPOLOGY

Parameter	Dual-Bridge Converter	Full-Bridge Converter
Voltage across the main switches	$V_i/2$	V_i
Average current through the main switches	$P_0/2V_i$	$P_0/2V_i$
Maximum current	$2\,P_0/V_i$	P_0/V_i
Maximum duty cycle	1	1

The average and rms currents through primary diodes D_{p1} and D_{p2} can be obtained from (30) and (31), shown at the bottom of this page, respectively

$$I_{Dp(\text{avg})} = \frac{V_i \cdot \alpha}{Z_0} \left[D + \frac{f_S}{f_0} \cdot \frac{3}{4\pi\alpha} \right]. \tag{30}$$

The average and rms currents through secondary diodes D_{s1} and D_{s2} can be obtained from (32) and (33), respectively

$$I_{Ds(\text{avg})} = \frac{\alpha \cdot nV_i}{2Z_0} \tag{32}$$

$$I_{Ds(\text{rms})} = \frac{\alpha \cdot nV_i}{2Z_0} \sqrt{1-D} + \frac{\alpha \cdot nV_i}{Z_0} \sqrt{D}. \tag{33}$$

The average and rms currents through cross diodes D_{c1}, D_{c2}, D_{c3}, and D_{c4} can be obtained from (34) and (35), respectively

$$I_{Dc(\text{avg})} = \frac{f_s}{f_0} \cdot \frac{V_i}{Z_0} \cdot \frac{\alpha^2 - 1}{2\pi} \tag{34}$$

$$I_{Dc(\text{rms})} = \frac{V_i}{Z_0} \cdot \sqrt{\frac{f_S}{f_0} \cdot \frac{(\alpha^2-1)\sqrt{\alpha^2-1}}{6\pi}}. \tag{35}$$

D. Converter Modeling

It can be seen from (23) that the commutation cell influences the converter gain in two ways. The first effect is proportional to the normalized conductance and causes a loss in the effective duty cycle. The second one is inversely proportional to the conductance and causes a gain in the effective duty cycle.

$$I_{Dp(\text{rms})} = \frac{\alpha V_i}{Z_0} \cdot \sqrt{D - \frac{f_S}{f_0} \cdot \left(\frac{1}{2\pi\alpha} - \frac{\alpha}{3\pi} + \frac{1}{4\pi} \sin^{-1}\left(\frac{1}{\alpha}\right) + \frac{(\alpha^2+2)\sqrt{\alpha^2-1}}{6\pi\alpha^2} \right)}. \tag{31}$$

TABLE II
COMPARISON BETWEEN THE PROPOSED CONVERTER, CONVENTIONAL INTERLEAVED TWO-SWITCH FORWARD CONVERTER, AND CONVENTIONAL DUAL-BRIDGE CONVERTER (ASSUMING ALL CONVERTERS WITH SAME INPUTS, OUTPUTS, AND POWER TRANSISTORS)

	Two-Switch Interleaved Forward Converter [31]	**Conventional Dual-Bridge Converter [19]**	**Double ZVS-PWM Active-Clamping Forward Converter [32]**	**Proposed Converter**
Input capacitors	1	2	2	2
Primary side main switches	4	4	2	4
Primary side auxiliary switches	0	0	2	2
Primary side diodes	4	4	4	8
Isolation transformers	2	1	1	1
Secondary side diodes	4	4	2	1
Secondary side inductors	2	1	2	1
Output capacitors	1	1	1	1
Voltage stress(es) across the input capacitor(s), considering $2{\cdot}V_i$ as the total input voltage	$2{\cdot}V_i$	V_i	V_i	V_i
Voltage stress across the primary side main switches considering $2{\cdot}V_i$ as the total input voltage	$2{\cdot}V_i$	V_i	$2{\cdot}V_i$	V_i
Current stress through the primary side main switches	I	I	I	I
Conduction losses on the primary side main switches	$4{\cdot}I^2{\cdot}R_{DS(on)}$	$2{\cdot}I^2{\cdot}R_{DS(on)}$	$2{\cdot}I^2{\cdot}R_{DS(on)}$	$2{\cdot}I^2{\cdot}R_{DS(on)}$
Transformer turns ratio	1:n	1:n	1:n	1:n

However, in practical designs, the first effect is much more significant than the second one. Only in very light load conditions (under 5% of the rated load current), the second term becomes more prominent. In fact, under such load condition, discontinuous conduction mode occurs and the gain in the effective duty loss is proportional to α. As a conclusion, the effect of the commutation can be modeled very nearly as a duty cycle loss proportional to the current or as a resistance in series with the output inductance as shown in Fig. 7.

The transfer function which allows the control of the output current is represented by (36). It must be mentioned that the resulting model is widely known in the literature and conventional controller design techniques can be used

$$\frac{I_0(s)}{d(s)} = \frac{V_i/n}{sL_0 + f_s(L_{r1} + L_{lkg})/n^2}. \tag{36}$$

E. Theoretical Comparison Between the Proposed Topology and the Conventional Full-Bridge Converter

In this section, a brief discussion comparing the proposed structure with the conventional full-bridge converter is presented. Table I shows that the voltage across the main switches in the dual-bridge structure is half the input voltage, but the maximum current value is twice that of the full-bridge converter. If MOSFET IRFP264 is used in the first structure and MOSFET IRFP460 is adopted in the second one, conduction losses for the dual-bridge and the full-bridge converters, represented as $P_{\mathrm{cond(DB)}}$ and $P_{\mathrm{cond(FB)}}$, respectively, can be given by

$$\begin{cases} P_{\mathrm{cond(DB)}} = 0.075 \cdot \left(\dfrac{2P}{V_i}\right)^2 = 0.3 \times \left(\dfrac{P}{V_i}\right)^2 \\ P_{\mathrm{cond(FB)}} = 0.27 \cdot \left(\dfrac{P}{V_i}\right)^2 = 0.27 \times \left(\dfrac{P}{V_i}\right)^2. \end{cases} \tag{37}$$

In this case, conduction losses for the full-bridge topology are 10% less than those for the dual-bridge converter. However, for a greater input voltage the opposite occurs, and the forward topology becomes the most attractive arrangement for high-power dc–dc conversion.

Another possibility lies is the use of a two single-switched forward converters. Then, the voltage across the main switches is equal to the input voltage as in the full-bridge converter. If the main switches are MOSFET, conduction losses are greater in the dual-bridge structure. Conduction losses are the same if insulated gate bipolar transistors (IGBTs) are used, although only two switches are used.

F. Comparison With Other Interleaved Topologies

To help design tradeoff and topology selection in engineering applications, the comparison between the proposed topology and other converters is necessary. Since it has two forward cells and it is suitable for high-power application, the conventional interleaved two-switch forward converter [31] and the topologies proposed in [19] and [32] are selected for this purpose due

TABLE III
DESIGN SPECIFICATIONS

Parameter	Value
Input voltage	V_i=350 V
Output voltage	V_0=50 V
Output power	P_0=2000 W
Switching frequency	f_s=100 kHz
Estimated leakage inductance	L_{lkg}=4 μH

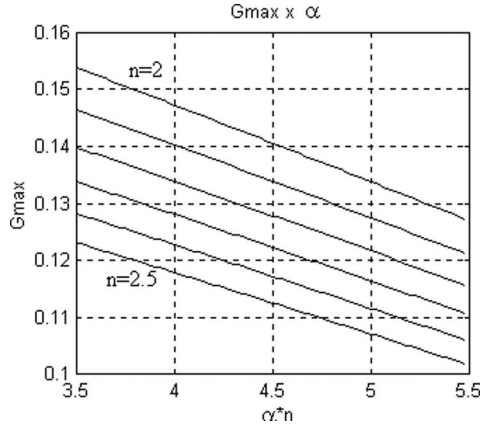


Fig. 8. Maximum static gain as a function of $\alpha{\cdot}n$, for $L_{lkg} = 4\ \mu$H.

to the similarity in structure and application, while others may not be suitable for comparison and are out of the scope of this paper. The comparison in Table II provides detailed design information and tradeoff for all three converters. It is clear that each converter has its advantages and disadvantages.

III. DESIGN EXAMPLE

A design example is presented in this section, considering the theoretical aspects described previously. The preliminary specifications are given in Table III.

A good choice for the resonance frequency is about ten times the switching frequency as the resonant elements must maintain the current peak as low as possible. They can be designed by limiting the maximum peak of the resonant current $I_{\mathrm{Sa(pk)}}$ to about one quarter of the load current referred to the primary side of the transformer

$$L_{r1} = L_{r2} \cong \frac{V_i}{40\pi f_s I_{\mathrm{Sa(pk)}}} = \frac{400}{40\pi \cdot 10^5 \cdot 5} = 6.3\,\mu\mathrm{H} \quad (38)$$

$$C_{r1} = C_{r2} \cong \frac{I_{\mathrm{Sa(pk)}}}{10\pi f_s V_i} = \frac{5}{10\pi \cdot 10^5 \cdot 400} = 3.9\,\mathrm{nF}. \quad (39)$$

It must be mentioned that (38) and (39) give the approximate values of the resonant elements. Then, one must choose the commercially available capacitor whose value is approximately equal to the calculated one, and considering the desired resonance frequency, the resonant inductor must be redesigned.

The next step in designing the proposed converter is to plot the curves shown in Fig. 6, but in this case considering the estimated leakage inductance. The required static gain is calculated using

TABLE IV
PARAMETERS SET USED IN THE PROTOTYPE

Parameter	Value
Total input voltage	$2{\cdot}V_i$=400 V
Output voltage	V_0=50 V
Output power	P_0=2000 W
Switching frequency	f_s=100 kHz
Input capacitors	C_1=C_2=1 mF
Resonant inductors	L_{r1}=L_{r2}=5 μH
Resonant capacitors	C_{r1}=C_{r2}=3.9 nF
Transformer	Core type: EE 65/33/26 Primary windings: 1 copper tape (27 × 0,15 mm) – 12 turns per winding Secondary windings: 2 copper tapes (27 × 0,15 mm) – 5 turns per winding
Primary inductances	L_{p1}=L_{p2}=1 mH
Secondary inductances	L_{s1}=L_{s2}=180 μH
Output filter inductance	L_0=20 μH
Output filter capacitance	C_0=10 μF
Main switches S_1, S_2, S_3, S_4	IRFP264
Auxiliary switches S_{a1}, S_{a2}	IRF740
Auxiliary diodes D_{a1}, D_{a2}	UF5404
Cross diodes D_{c1}, D_{c2}, D_{c3}, D_{c4}	UF5404
Primary diodes D_{p1}, D_{p2}	MUR1560
Secondary diodes D_{s1}, D_{s2}	APT30D60B

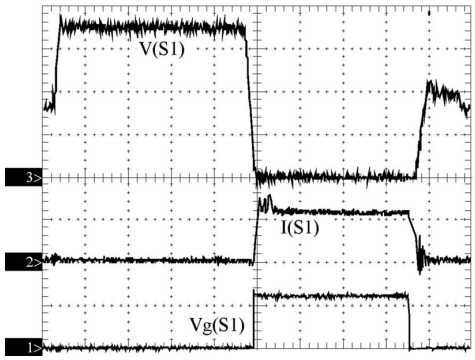


Fig. 9. Drain–source voltage, drain current, and gating signal of main switch S_1. Scales: V_{S1}—50 V/div; $V_{g(S1)}$—10 V/div; I_{S1}—10 A/div; time—1 μs/div.

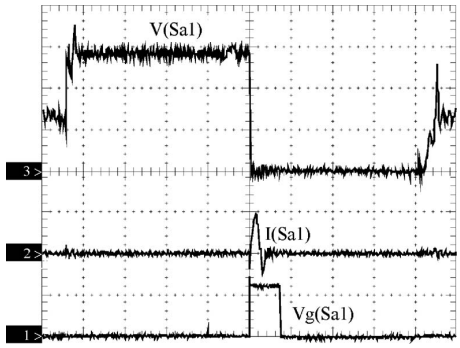


Fig. 10. Drain-source voltage and drain current, and gating signal of auxiliary switch S_{a1}. Scales: V_{Sa1}—100 V/div; $V_{g(Sa1)}$ —10 V/div; I_{Sa1}—5 A/div; time—1 μs/div.

(20) and parameter $\alpha{\cdot}n$ is obtained from (1) as follows:

$$G_{\max} = \frac{50}{350} = 0.14 \quad (40)$$

$$\alpha \cdot n = \frac{I_0}{V_i} \cdot \sqrt{\frac{L_{r1}}{C_{r2}}} = \frac{40}{350} \cdot \sqrt{\frac{5 \cdot 10^{-6}}{3.9 \cdot 10^{-9}}} = 4.09. \quad (41)$$

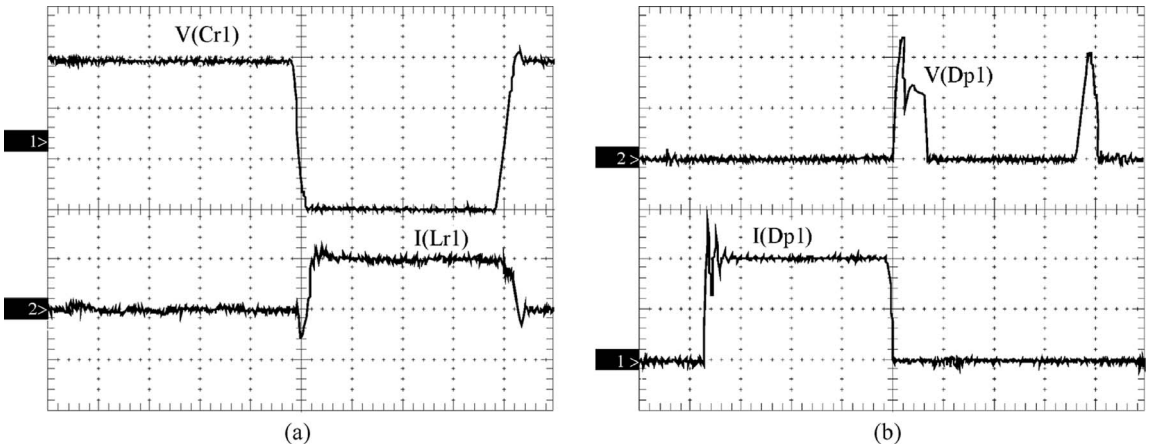


Fig. 11. (a) Resonant tank waveforms. Scales: V_{Cr1}—100 V/div; I_{Lr1}—20 A/div; time—1 μs/div (b) Voltage and current waveforms of diode D_{p1}. Scales: V_{Dp1}—100 V/div; I_{Dp1}—10 A/div; time—1 μs/div.

According to Fig. 8, it can be seen that n must be less than 2.1. A comparison between Figs. 6 and 8 shows the relevance of considering the leakage inductance. From Fig. 8, it can be seen that n must be about 2.5, what would cause the output voltage to be lower than the desired value. The average current through main switches S_1 and S_2 can be estimated by (42) and the voltage across them is V_i. The average current through diodes D_{p1} and D_{p2} is approximately equal to the current flowing though the auxiliary switch I_{Sa}. The voltage across them is ideally V_i, but the blocking voltage must be V_i due to the reverse recovery current

$$I_{S(\text{avg})} \cong \frac{P_i}{V_i} \tag{42}$$

where P_i is the input power.

Auxiliary switches S_{a1} and S_{a2}, as well as the respective series diodes D_{a1} and D_{a2}, are supposed to have the same blocking voltage as diodes D_{p1} and D_{p2} and the current through them is equal to the resonant current.

Output diodes D_{s1} and D_{s2} conduct half the output current and the respective blocking voltage is twice the voltage across each primary winding. However, the blocking causes high ripple voltage and a snubber is necessary, what also occurs in the full-bridge converter [33].

The output filter can be normally designed for twice the switching frequency, as explained before. Input capacitors C_1 and C_2 are supposed to minimize the high frequency ripple and can be calculated by [34]

$$C_1, C_2 \geq \frac{2 \cdot I_0 \cdot D_{\max} \cdot T_s}{n}. \tag{43}$$

It is also important to mention that unbalance between the voltages across input capacitors C_1 and C_2 tends to be small due to the constructive differences between the primary windings, since energy transfer between them may occur through the cross diodes.

To specify cross diodes D_{c1}, D_{c2}, D_{c3}, and D_{c4}, the transformer ratio between the primary windings is considered unity, and these diodes must conduct only the remaining leakage energy. The blocking voltage must be higher than V_i.

IV. Experimental Results

An experimental prototype was implemented with the parameters set considered in the design example shown in the previous section and given in Table IV. It must be mentioned that the transformer is designed as in the case of the push–pull converter [1]. The leakage inductance was experimentally measured, being equal to 4 μH. It must also be mentioned that the experimental results discussed later are obtained under the operating conditions stated in Table IV.

Fig. 9 shows that the switch S_1 is turned on and off under zero-voltage condition. Some oscillation can be seen in the drain–source voltage waveform. It occurs because the cross diodes do not assume the current instantly [35], and is also due to the reverse recovery of the antiparallel diodes of the main switches.

The waveforms regarding auxiliary switch S_{a1} are shown in Fig. 10. Turning-on occurs in ZCS mode, and the switch is turned off under ZCZVS condition. Some oscillation can be noticed at the moment when switches S_3 and S_4 are turned on. They are due to the charging of the intrinsic capacitance of the auxiliary switch and can be minimized by using snubbers.

Fig. 11(a) presents the voltage across the resonant capacitor and the current through the resonant inductor. It must be mentioned that reactive energy flows during only 10% of the switching period. Therefore, soft switching is achieved with almost null voltage. Fig. 11(b) represents the current and voltage waveforms regarding primary diode D_{p1}. It can be seen that the snubber limits the voltage peak caused by the reverse recovery current.

Fig. 12 shows the voltage across secondary diode D_{s2}. The reverse recovery of the diode causes oscillations, even with soft commutation on the primary side, demanding the use of snubbers.

Finally, Fig. 13 represents the efficiency as a function of the output power for the soft-switched converter operating at 100 kHz. Measured efficiency at rated load is about 93%. It tends to be less at light load condition since the amount of

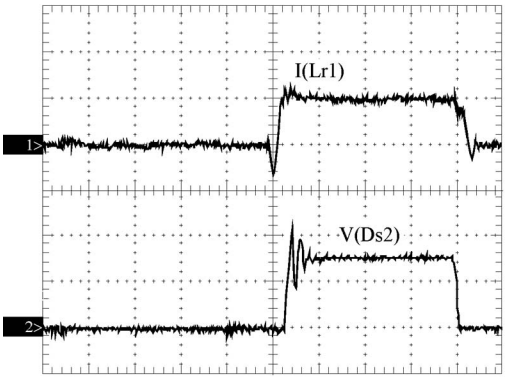


Fig. 12. Voltage across secondary diode D_{s2} and current through resonant inductor L_{r1}. Scales: V_{Ds2}—100 V/div; I_{Lr1}—20 A/div; time—1 μs/div.

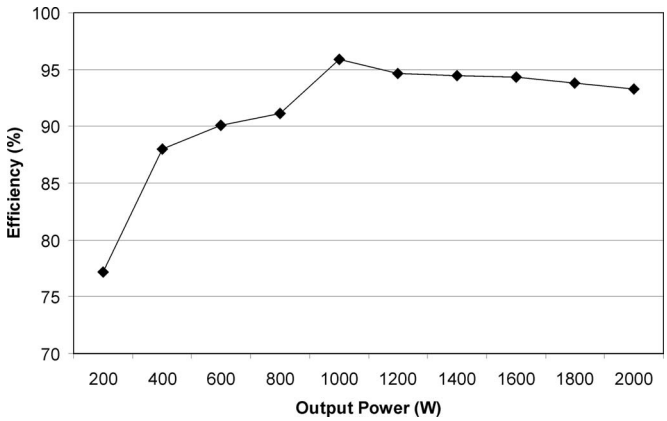


Fig. 13. Efficiency curve.

circulating reactive energy is constant. However, efficiency is improved at rated load because the duty cycle loss is less than that in [21] and [23] due to the small series inductance. In low duty cycle condition, efficiency tends to be greater due to the small series inductance.

V. Conclusion

This paper has proposed a soft-switching dc–dc converter that can be used in high-voltage and/or high-power applications. The theoretical study and experimental results have shown its functionality and viability for high-power conversion.

Although the dual-bridge structure presents higher rms currents through the main switches, with the voltages across them being equal to half those across the switches of a full-bridge converter, MOSFETs with reduced voltage rating and on-resistance can be employed to provide lower conduction losses. If the same IGBT is used in the dual-bridge and full-bridge converters, conduction losses will tend to be the nearly the same in both converters. For input voltages higher than 500 or 600 V, conduction losses in the dual-bridge topology become lower.

In front of the study developed in this paper, the following prominent advantages can be addressed to the topology: reduced blocking voltage across the switches if compared with full bridge structures; improved use of the capacity of the high frequency transformer if compared with conventional forward converters; there are no additional voltage and/or current stresses in the main semiconductor devices; high efficiency, since the soft switching cell requires a small amount of energy; soft switching is achieved in all active switches for the entire load range; design procedure is rather simple; parallelism of several structures is possible.

References

[1] Y. Gu, Z. Lu, Z. Qian, X. Gu, and L. Hang, "A novel ZVS resonant reset dual switch forward dc–dc converter," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 96–103, Jan. 2007.

[2] T.-F. Wu, J.-C. Hung, J.-T. Tsai, C.-T. Tsai, and Y.-M. Chen, "An active-clamp push–pull converter for battery sourcing applications," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 196–204, Jan. 2008.

[3] L. Yan and B. Lehman, "Integrated magnetic full wave converter with flexible output inductor," *IEEE Trans. Power Electron.*, vol. 18, no. 2, pp. 670–678, Mar. 2003.

[4] J. Sun, K. F. Webb, and V. Mehrotra, "Integrated magnetics for current-doubler rectifiers," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 582–590, May 2004.

[5] T. Qian and B. Lehman, "Coupled input-series and output-parallel dual interleaved flyback converter for high input voltage application," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 88–95, Jan. 2008.

[6] T. Jin, K. Zhang, K. Zhang, and K. M. Smedley, "A new interleaved series input parallel output (ISIPO) forward converter with inherent demagnetizing features," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 888–895, Mar. 2008.

[7] W.-J. Lee, C.-E. Kim, G.-W. Moon, and S.-K. Han, "A new phase-shifted full-bridge converter with voltage-doubler-type rectifier for high-efficiency PDP sustaining power module," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2450–2458, Jun. 2008.

[8] A. J. Mason, D. J. Tschirhart, and P. K. Jain, "New ZVS phase shift modulated full-bridge converter topologies with adaptive energy storage for SOFC application," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 332–342, Jan. 2008.

[9] X. Ruan and Y. Yan, "Soft-switching techniques for PWM dc/dc full-bridge converters," in *Proc. Power Electron. Spec. Conf.*, 2000, pp. 634–639.

[10] X. Ruan and Y. Yan, "A novel zero-voltage and zero-current-switching PWM full bridge converter using two diodes in series with the lagging leg," *IEEE Trans. Ind. Electron.*, vol. 48, no. 4, pp. 777–785, Aug. 2001.

[11] W. Chen, X. Ruan, and R. Zhang, "A novel zero-voltage-switching PWM full bridge converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 793–801, Mar. 2008.

[12] X. Ruan and B. Li, "Zero-voltage and zero current switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 213–220, Feb. 2005.

[13] X. Wu, X. Xie, J. Zhang, R. Zhao, and Z. Qian, "Soft switched full bridge dc–dc converter with reduced circulating loss and filter requirement," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1949–1955, Sep. 2007.

[14] Y. Jang and M. M. Jovanovic, "A new PWM ZVS full-bridge converter," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 987–994, May 2007.

[15] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov. 1992.

[16] W. Song and B. Lehman, "Dual-bridge dc–dc converter: a new topology characterized with no deadtime dc–dc converters," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 94–103, Jan. 2004.

[17] W. Chen and X. Ruan, "Zero-voltage-switching PWM hybrid full-bridge three-level converter with secondary-voltage clamping scheme," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 644–654, Feb. 2008.

[18] G. G. Oggier, G. O. Garcıa, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1826–1838, Jul. 2009.

[19] N. H. Kutkut, G. Luckjiff, and D. M. Divan, "A dual bridge high current dc-to-dc converter with soft switching capability," in *Proc. IEEE Ind. Appl. Soc. Ann. Meeting*, 1997, vol. 2, pp. 1398–1405.

[20] X. Liang, H. Wei, and X. Ruan, "An interleaved three-level forward converter-suitable for the application of voltage regulator module (VRM)," in *Proc. Power Electron. Spec. Conf.*, 2003, vol. 1, pp. 127–131.

[21] D. Xu, M. Chen, J. Lou, and M. Luo, "Transformer secondary leakage inductance based ZVS dual bridge dc/dc converter," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1408–1416, Nov. 2004.
[22] N. H. Kutkut, "A new dual-bridge soft-switching dc-to-dc power converter for high power applications," in *Proc. Ind. Electron. Conf. Records*, 1999, vol. 1, pp. 474–479.
[23] R. Torrico-Bascopé and I. Barbi, "Dual-bridge dc–dc converter with soft switching features," in *Proc. Appl. Power Electron. Conf. Expo.*, 2001, vol. 2, pp. 722–727.
[24] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc–dc converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.
[25] W. Song and B. Lehman, "Current-fed dual-bridge dc–dc converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 461–469, Mar. 2007.
[26] L. C. Freitas, V. J. Farias, P. S. Caparelli, J. B. Vieira, Jr., H. L. Hey, and D. F. Cruz, "An optimum ZVS-PWM dc–dc converter family: analysis, simulation and experimental results," in *Proc. IEEE Power Electron. Spec. Conf.*, 1992, pp. 229–235.
[27] L. C. Freitas and P. R. C. Gomes, "A high-power high-frequency ZCS-ZVS-PWM buck converter using a feedback resonant circuit," *IEEE Trans. Power Electron.*, vol. 10, no. 1, pp. 19–24, Jan. 1995.
[28] K. M. Smith, Jr. and K. M. Smedley, "Properties and synthesis of lossless, passive soft switching converters," in *Proc. 1st Int. Congr. Israel Energy Power Motion Control*, May 1997, pp. 112–119.
[29] A. J. Nascimento, Jr., L. C. Freitas, V. J. Farias, and J. B. Vieira, Jr., "PWM control for parallel converters in the current sharing mode," in *Proc. 8th Eur. Conf. Power Electron. Appl.*, 1999, pp. 293–297.
[30] C. Q. Lee, K. Siri, and T. F. Wu, "Dynamic current distribution controls of a parallel connected converter system," in *Proc. Power Electron. Spec. Conf. (PESC'91)*, 1991, vol. I, pp. 875–881.
[31] F. D. Tan, "The forward converter: From the classic to the contemporary," in *Proc. 17th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2002, pp. 857–863.
[32] R. Torrico-Bascopé and I. Barbi, "A double ZVS-PWM active-clamping forward converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 745–751, Nov. 2001.
[33] M. Brunoro and J. L. F. Vieira, "A high-performance ZVS full-bridge dc–dc 0–50 V/0–10 A power supply with phase shift control," *IEEE Trans. Power Electron.*, vol. 14, no. 3, pp. 495–505, May 1999.
[34] A. I. Pressman, *Switching Power Supply Design*, 2nd ed. New York: McGraw-Hill, 1998.
[35] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. Hoboken, NJ: Wiley, 2003.

Demercil de Souza Oliveira, Jr. was born in Santos, São Paulo, Brazil, in 1974. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1999 and 2001, respectively, and the Ph.D. degree from the Federal University of Santa Catarina, Florianopolis, Santa Catarina, Brazil, in 2004.

Currently, he is a Researcher in the Group of Power Processing and Control, and a Professor since 2004 at the Federal University of Ceará, Ceará, Brazil. His research interests include static power converters, soft commutation, and renewable energy applications.

Carlos Elmano de Alencar e Silva was born in Ceará, Brazil, in 1981. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Ceará, Ceará, Brazil, in 2004 and 2007, respectively.

Currently, he is a Professor at the Federal University of Ceará. His research interests include dc–dc conversion, dc–ac conversion, and digital control.

René Pastor Torrico-Bascopé received the B.Sc. degree in electrical engineering from San Simón University, Cochabamba, Bolivia, in 1992, and the M.Sc. and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Santa Catarina, Brazil, in 1994 and 2000, respectively.

He is currently a Professor in the Department of Electrical Engineering, Federal University of Ceará, Fortaleza, Ceará, Brazil. His main research interests include power supplies, power factor correction techniques, uninterruptible power systems, and renewable energy systems.

Fernando Lessa Tofoli was born on March 11, 1976, in São Paulo, Brazil. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1999, 2002, and 2005, respectively.

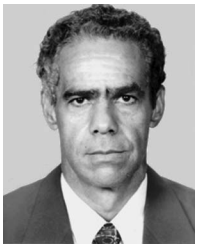
Currently, he is a Professor at the Federal University of São João del-Rei, São João del-Rei, Brazil. His research interests include power-quality-related issues, high-power factor rectifiers, and soft switching techniques applied to static power converters.

Carlos Augusto Bissochi, Jr. received the B.Sc. degree in electrical engineering from the State University of São Paulo, Brazil, in 1994, and the M.Sc. and Ph.D. degrees in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1997 and 2003, respectively.

Currently, he is a Professor at the Federal University of Uberlândia, Uberlândia, Brazil. His research interests include soft switching, novel converter topologies, ac–ac audio amplifiers, and electrical motor drives.

João Batista Vieira, Jr. was born in Panamá, Brazil, in 1955. He received the B.Sc. degree in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1980, and the M.Sc. and Ph.D. degrees from the Federal University of Santa Catarina, Florianópolis, Santa Catarina, Brazil, in 1984 and 1991, respectively.

In 1980, he became an Instructor in the Electrical Engineering Department, Federal University of Uberlândia, where he is currently a Professor. He has published more than 250 papers. His research interests include high-frequency power conversion, modeling and control of converters, power-factor-correction circuits, and new converter topologies.



Valdeir José Farias was born in Araguari, Brazil, in 1947. He received the B.Sc. degree in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1975, the M.Sc. degree in power electronics from the Federal University of Minas Gerais, Belo Horizonte, Brazil, in 1981, and the Ph.D. degree from the State University of Campinas, Campinas, Brazil, in 1989.

He is currently a Professor of Electrical Engineering at the Federal University of Uberlândia. He has published more than 250 papers. His research interest includes power electronics, in particular, soft-switching converters and active power filters.

Luiz Carlos de Freitas was born in Brazil, in 1952. He received the B.Sc. degree in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1975, and the M.Sc. and Ph.D. degrees from the Federal University of Santa Catarina, Florianópolis, Santa Catarina, Brazil, in 1985 and 1992, respectively.

He is currently a Professor of Electrical Engineering at the Federal University of Uberlândia. He has published more than 250 papers and has two Brazilian patents pending. His research interests include high-frequency power conversion, modeling and control of converters, power-factor-correction circuits, and new converter topologies.