A UPS With 110-V/220-V Input Voltage and High-Frequency Transformer Isolation

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***Abstract*—This paper proposes an isolated double-conversion uninterruptible power system with power factor correction using a high-frequency transformer and with input voltages equal to 110 V/220 V. The arrangement is suitable to rack-type structures because it has a small size and a reduced weight. For both input voltages, the proposed converter has almost the same efficiency processing the same output power. Other relevant features include soft commutation of the controlled switches in the chopper and boost stages, a simple control strategy that can be implemented with well-known integrated circuits, and the use of few batteries in series due to the step-up stage. Qualitative analysis and experimental results obtained with a 2-kVA prototype show a normal efficiency of over 86% for the worst case of input voltage and an input power factor of over 99%.**

***Index Terms*—Double-conversion uninterruptible power system (UPS), high-frequency transformer, power factor correction (PFC), soft commutation.**

I. Introduction

NOWADAYS, uninterruptible power systems (UPSs) are used to protect sensitive loads against a wide variety of utility voltage disturbances and power outages. Most of such systems consist in the true online UPS configuration. In general, this is the most reliable UPS configuration due to its simplicity and the continuous charge of the batteries, which means that they are always ready for the next power outage. This kind of UPS provides total independence between input and output voltage amplitude and frequency, and thus, high output voltage quality can be obtained [1].

Most of the true online UPSs operate with a low-frequency transformer using a silicon-steel core. In this configuration, an isolating transformer is normally required for proper operation of the bypass circuit and also to improve reliability of the system, since the transformer offers galvanic isolation to the load from undesirable disturbances of the main supply [2]. Such a transformer is placed at the input or output depending on the topology arrangement. The addition of such magnetic component increases both weight and volume and also adds cost and difficulties in the transportation to the installation site.

Transformerless UPS incorporating a common neutral bus line could be a solution to improve power conversion efficiency and volume and weight reduction [3], [4]. Although this UPS topology offered a way to obtain these advantages, this type is more susceptible to interference from spikes and transients caused by assorted devices connected to the utility grid [5].

During the 1990s, the evolution of semiconductors (i.e., diodes and transistors) and other components has allowed the development of devices with nearly ideal characteristics, making the research on UPSs with high-frequency transformers possible and very attractive due to its weight and volume reduction. Several UPS topologies with this newly introduced characteristic have been proposed in [6]–[12]. Some of them are analyzed and discussed here as follows.

The UPS topology shown in Fig. 1 was studied in [6]. It consists of a power factor correction (PFC) current-fed full-bridge converter and a voltage-source full-bridge inverter. In this circuit, hard commutation of the controlled switches compromises efficiency, and several batteries placed in series are necessary to achieve high dc-link voltage. In addition, the current drawn by the battery bank is pulsed, affecting the reliability of the battery set.

The UPS shown in Fig. 2 was studied in [7]. The circuit is composed of a modified PFC current-fed full-bridge structure and a voltage-source full-bridge inverter, which is similar to the previous one. This topology has the advantages of a reduced amount of semiconductors in series during power transfer, implying the reduction of conduction losses and improving efficiency. The disadvantages include hard commutation of the controlled switches and many batteries in series needed to achieve high dc-link voltage in order to supply the voltage-source inverter.

Fig. 3 shows the series–parallel resonant system proposed in [8]. It presents the galvanic isolation between the input side, the output side, and the battery. This system has the advantages of PFC, single preregulator stage, soft commutation of the controlled switches, and few batteries in series. On the other hand, the disadvantages are the complex control strategy and the adjustment of resonant parameters.

The two-stage UPS studied in [9] is shown in Fig. 4. The first stage consists of a PFC-DCM flyback converter with an integrated battery charger, and the second stage is a boost inverter. Due to the operation of the flyback converter in discontinuous conduction mode, the system is only suitable for low-power applications, i.e., below 500 W.

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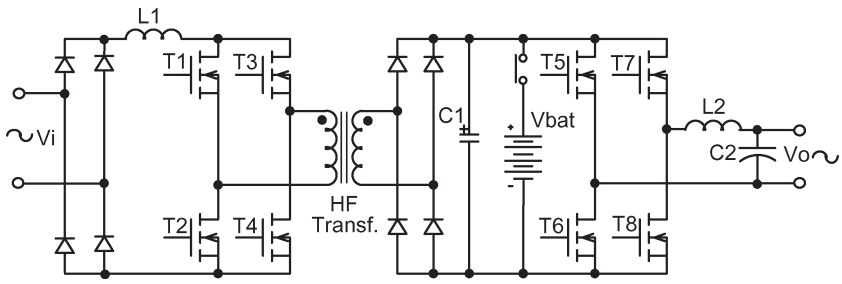

Fig. 1. Switched-mode PFC rectifier with high-frequency transformer for a single-phase UPS proposed in [6].

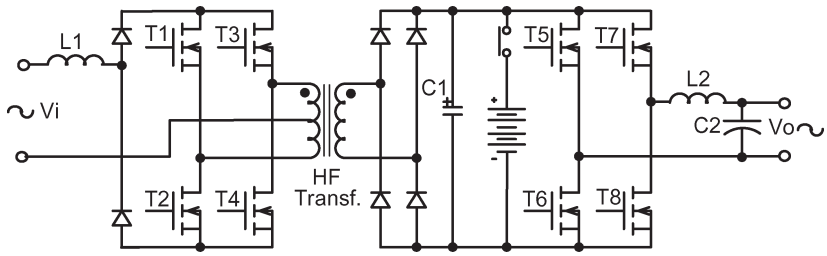

Fig. 2. High-frequency isolation UPS with novel SMR proposed in [7].

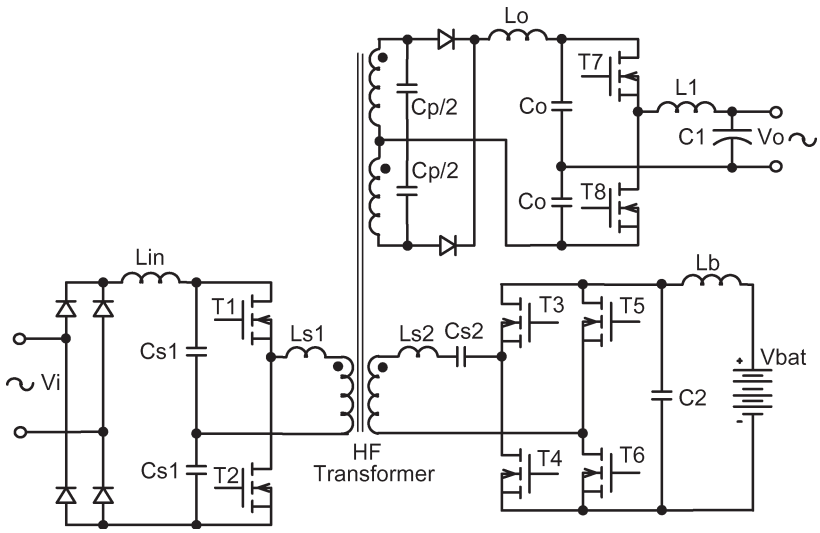

Fig. 3. Series–parallel resonant converter UPS proposed in [8].

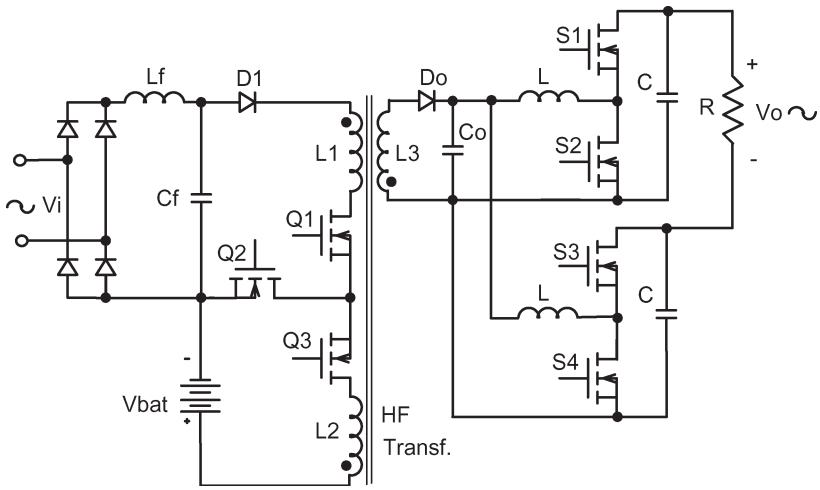

Fig. 4. Two-stage UPS proposed in [9].

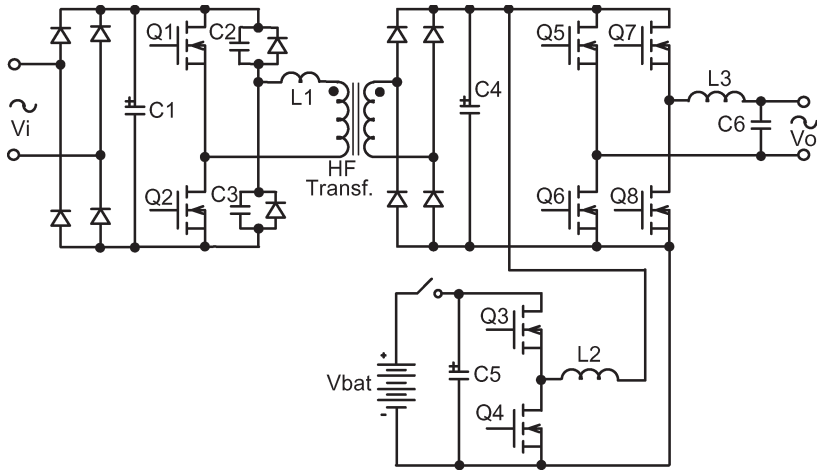

Fig. 5. Unity power factor single-phase UPS proposed in [10].

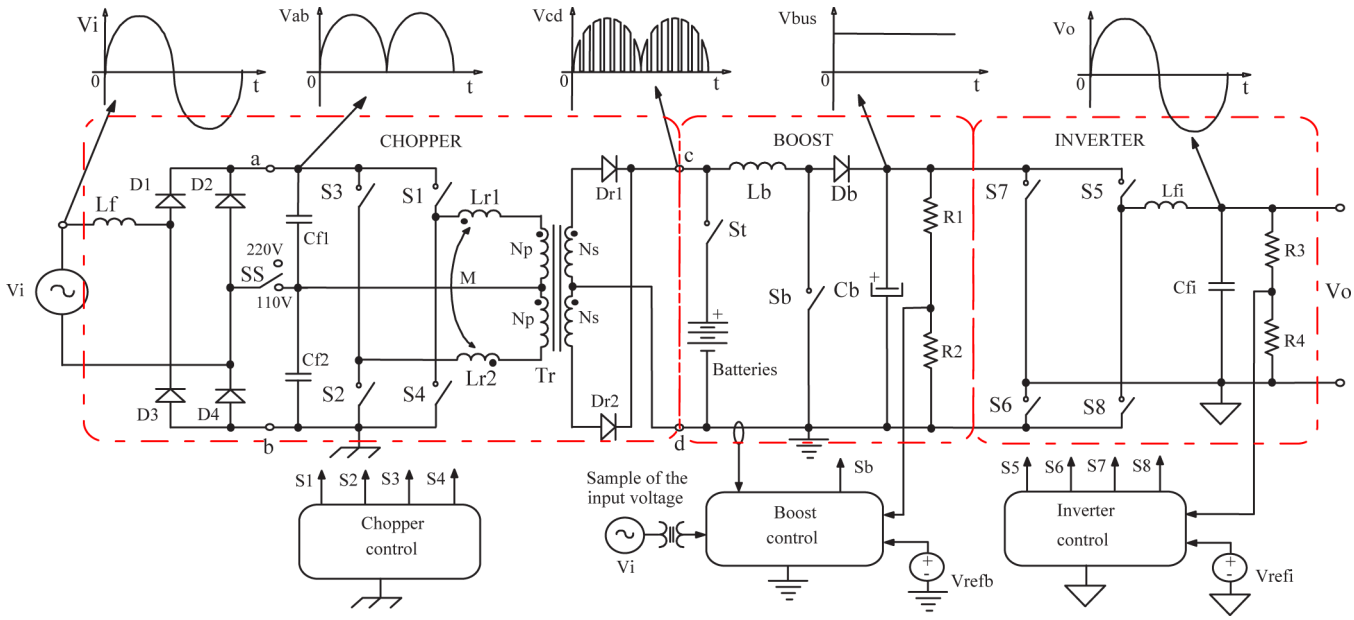

Fig. 6. Proposed single-phase high-frequency isolated UPS.

Fig. 5 shows the detailed diagram of the UPS reported in [10]. The circuit consists basically of a zero-current-switching-controlled partial series-resonant dc–dc converter, a dynamic power compensator given by a bidirectional converter, and a voltage-source full-bridge inverter. Advantages of the circuit include PFC, soft commutation of the switches in the input stage, and the inverter switches operating at 50 Hz. The main disadvantage lies in the need of several batteries in series to achieve the adequate dc-link voltage when the battery bank supplies the load, since the bidirectional converter operation is analogous to a buck topology.

Some other works involving isolated preregulators were proposed in other conference proceedings [11], [12] and also could be used as the input stage of high-frequency isolated UPSs.

According to the analysis of drawbacks related in the aforementioned UPS topologies, a feasible high-frequency transformer isolation UPS is proposed in this paper.

This proposal, as shown in Fig. 6, consists of a flexible UPS topology, which allows the UPS operation for a wide-range input voltage (110 V/220 V). It is also important to emphasize that it could operate with two input voltage levels without compromising the global efficiency, which is almost the same for both input voltage levels.

The adopted control strategy is simple. The three stages are controlled by using well-known conventional pulsewidth-modulation (PWM) control techniques, allowing the use of low-cost commercial integrated circuits. The major drawback of this proposal is the number of power processing stages that affects its efficiency.

The preregulator topology, which is composed of chopper and boost stages, presents soft commutation of the switches, and few batteries in series are needed due to eventual voltage unbalance across them when several units are connected in series. Other features such as isolation and PFC are the former advantages of the aforementioned systems.

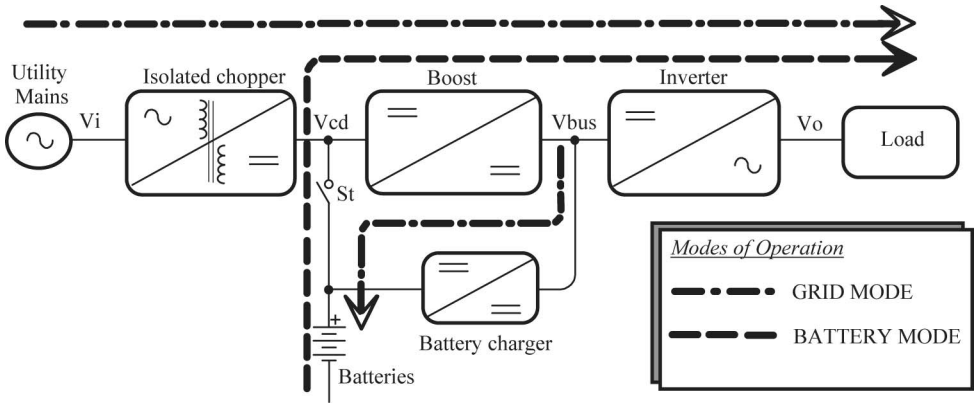

Fig. 7. Simplified block diagram of the proposed single-phase high-frequency isolated UPS.

In this UPS topology, the bypass circuit operation is optional. This feature is commonly not used for high-frequency UPS solutions. Thus, to improve reliability, the $N+1$ module redundancy parallel operation is recommended.

The operation with two input voltage levels, the cascaded operation of the chopper and boost stages, and the possibility of achieving soft commutation of the chopper switches using coupled inductors were achieved in [7] and [14]–[17].

II. Proposed UPS Circuit

A. Topology Description

The proposed UPS is shown in Fig. 6. It is composed of the following parts: an isolated chopper comprising of the rectifier diodes D_1-D_4; a high-frequency input filter comprising of the inductor $L_{\rm f}$ and capacitors $C_{\rm f1}$ and $C_{\rm f2}$; a controlled full bridge comprising of the switches S_1-S_4, a high-frequency transformer $T_{\rm r}$, coupled inductors $L_{\rm r1}-L_{\rm r2}$, and rectifier diodes $D_{\rm r1}-D_{\rm r2}$; a traditional boost converter comprising of the inductor $L_{\rm b}$, switch $S_{\rm b}$, diode $D_{\rm b}$, and capacitor $C_{\rm b}$; a full-bridge voltage-source inverter comprising of the switches S_5-S_8; and the output filter formed by inductor $L_{\rm fi}$ and capacitor $C_{\rm fi}$. In addition, the waveforms corresponding to the operation of each stage are indicated in this figure.

B. Modes of Operation

The operation of the proposed UPS can be divided into two modes, as shown in Fig. 7: the grid mode, which is also sometimes referred to as normal mode, and the battery-powered mode.

1) Grid Mode: During the normal mode, i.e., under the condition in which there is no power failure or the utility is at least 85% of its rated operating condition, the isolated chopper stage, boost stage, inverter stage, and battery charger circuit are operating. In accordance with the utility voltage level, an automatic detector sets the UPS for the proper input voltage. For utility voltage of 220 $V_{\rm ac}$, the selector switch (SS) should be set to position 220 V. On the other hand, if the utility voltage is 110 $V_{\rm ac}$, the SS should be switched to position 110 V.

The detailed principle of operation for each stage is shown in the following sections.

2) Battery-Powered Mode: When the supervisory circuit detects an ac line failure, the isolated chopper stage is turned off and switch S_t turns on, transferring the input of the boost stage from the isolated chopper to the battery bank for boost dc/dc operation. In this operating mode, the battery charger circuit is disabled. During this transition, the $V_{\rm bus}$ capacitors were designed to provide sufficient energy to the inverter, whereas the battery bank is not connected.

When the supervisory circuit detects ac line voltage reestablishment in normal operating ranges, the isolated chopper stage is turned on, whereas the boost converter control and the inverter control are synchronized with the input voltage.

III. Analysis of the Chopper Operation With Input Voltage Equal to 110 V

A. Principle of Operation

The chopper operates with a fixed duty cycle $(D \cong 0.5)$ using IC UC3525A. The control strategy allows the application of high-frequency voltage pulses to the primary windings of transformer $T_{\rm r}$, enabling the use of a high-frequency transformer.

When the input voltage is 110 V, the SS (manual or automatic) must be turned on and adjusted to the 110-V position point. Under this condition, diodes D_2 and D_4 are always reverse biased.

Considering the positive semicycle of the input voltage, during half of the switching period, the converter operation can be resumed to four stages, as shown in Fig. 8, as the relevant waveforms are shown in Fig. 9. The operation of the topology in the negative semicycle is analogous.

Interval (t_0-t_1): At $t=t_0$, switches S_1 and S_2 are turned on. The input voltage charges inductor $L_{\rm r1}$, and the current increases linearly from zero to $nI_{\rm Lb}$. The output current $I_{\rm Lb}$ is freewheeling.

Interval (t_1-t_2): During this interval, energy is transferred from the input source V_i to the load, represented by current source $I_{\rm Lb}$.

Interval (t_2-t_3): At $t=t_2$, switches S_1 and S_2 are turned off under zero-voltage condition due to the intrinsic

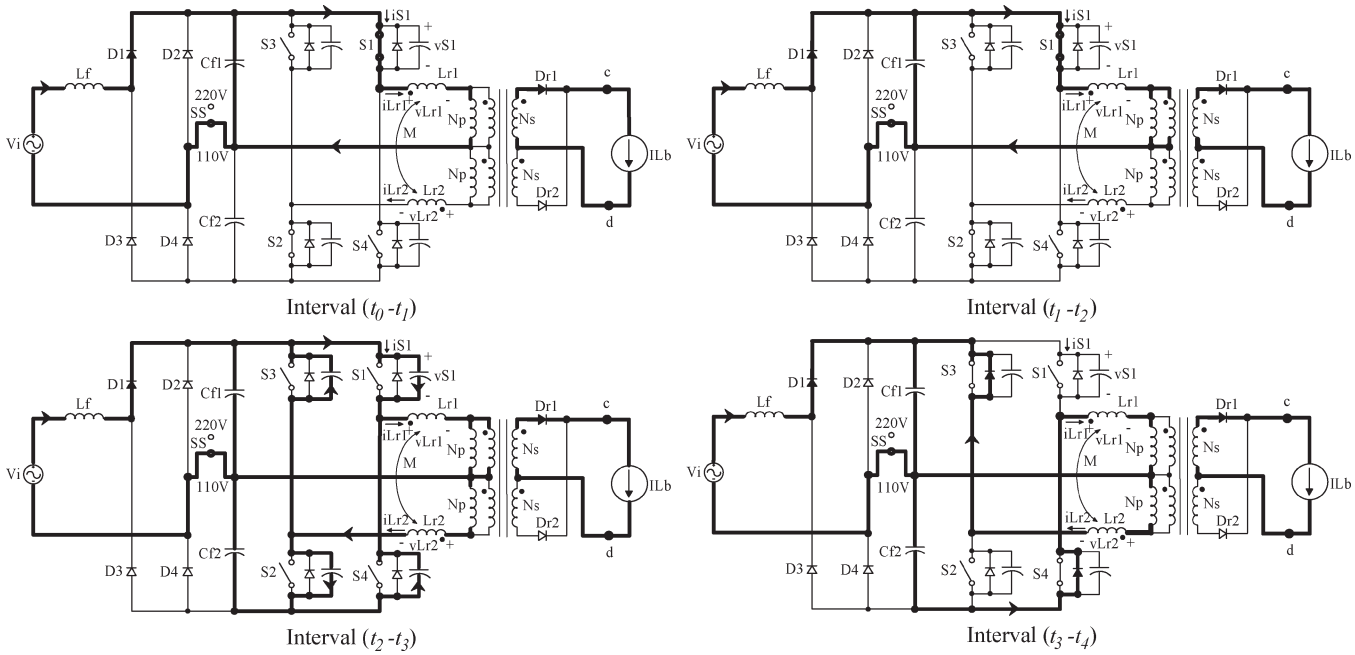

Fig. 8. Operating stages of the chopper circuit when the input voltage is 110 V.

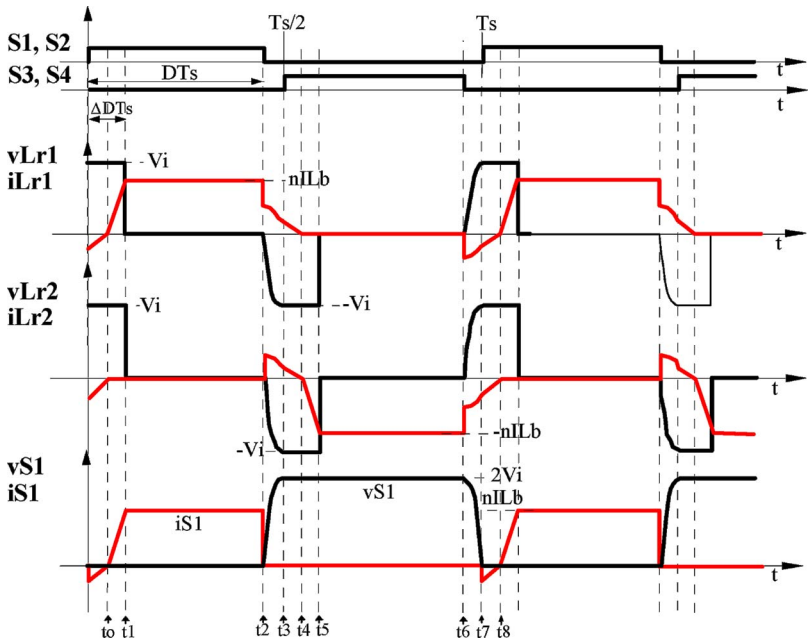

Fig. 9. Main theoretical waveforms when the input voltage is 110 V.

capacitances. Half of the energy stored in inductor L_{r1} is transferred to inductor L_{r2}. The intrinsic capacitances are then charged and discharged.

Interval (t_3–t_4): When the voltage across switches S_1 and S_2 is equal to V_i, the antiparallel diodes of switches S_3 and S_4 are directly biased. During this interval, switches S_3 and S_4 must be turned on.

When the input voltage is 110 V, the input current is twice that in 220 V, so that the same output power is maintained. As one can see in Fig. 8, only one controlled switch of the chopper is involved during the energy transfer, and consequently, conduction losses are reduced.

In the chopper stage, duty-cycle reduction ΔD occurs due to the input voltage across commutation inductors L_{r1} and L_{r2} and also to the transformer leakage inductances, which cause the linear variation of the current through them. During this interval, the output current I_{Lb} is freewheeling through rectifier diodes D_{r1} and D_{r2}. Therefore, there is no power transfer from the input to the load.

The duty-cycle reduction can be obtained from the inductor voltage given by

$$v_L = L\frac{\Delta i_L}{\Delta t} \tag{1}$$

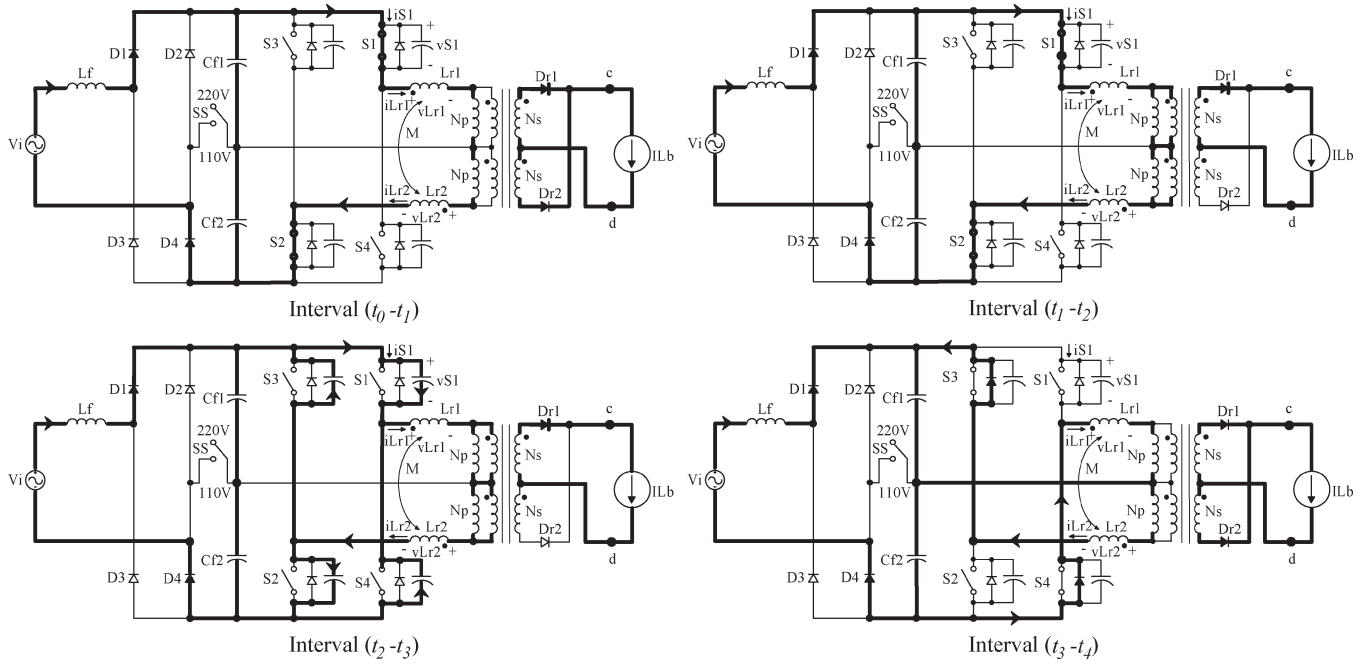

Fig. 10. Operating stages of the chopper circuit when the input voltage is 220 V.

as the involved parameters are

$$v_L = \left|V_{i(\mathrm{pk})_{110\,\mathrm{V}}} \sin(\theta)\right| \tag{2}$$

$$\Delta i_L = \left|2nIL_{b(\mathrm{pk})} \sin(\theta)\right| \tag{3}$$

$$\Delta t = \Delta D T_\mathrm{s} \tag{4}$$

$$L = L_{\mathrm{r}1} = L_{\mathrm{r}2} \tag{5}$$

where n is the transformer turns ratio, $IL_{b(\mathrm{pk})}$ is the peak current through the boost inductor, $V_{i(\mathrm{pk})}$ is the peak input voltage, $\theta = \omega t$ is the phase angle of the input voltage, and T_s is the switching period.

Substituting (2)–(5) in (1) results in the following expression:

$$\Delta D = \frac{2L_{\mathrm{r}1} f_\mathrm{s} n IL_{b(\mathrm{pk})} \sin(\theta)}{V_{i(\mathrm{pk})_{110\,\mathrm{V}}} \sin(\theta)} \tag{6}$$

where f_s is the switching frequency.

The rms output voltage of the chopper, which supplies the boost converter, is given by

$$V_{\mathrm{cd(rms)}} = \sqrt{\frac{1}{\pi}\int_0^\pi 2(D-\Delta D)\left(nV_{i(\mathrm{pk})_{110\,\mathrm{V}}} \sin(\theta)\right)^2 d\theta}. \tag{7}$$

Simplifying (7) yields

$$V_{\mathrm{cd(rms)}} = nV_{i(\mathrm{pk})_{110\,\mathrm{V}}} \sqrt{(D-\Delta D)} \tag{8}$$

where $V_{\mathrm{cd(rms)}}$ is the chopper rms output voltage and D is the duty cycle. The inductor peak current is calculated with

$$I_{\mathrm{Lb(pk)}} \cong \frac{\sqrt{2}P_\mathrm{o}}{V_{\mathrm{cd(rms)}}} \tag{9}$$

where P_o is the UPS active output power.

IV. Analysis of the Chopper Operation With Input Voltage Equal to 220 V

A. Principle of Operation

In this mode, the SS must be set to 220-V position. The control strategy is the same one used when the input voltage is 110 V.

Considering the positive semicycle of the input voltage, during half of the switching period, the converter operation can be represented by four stages, as shown in Fig. 10, where the theoretical waveforms are shown in Fig. 11. The description of the operation is similar to the case where the input voltage is 110 V.

Although the current flows simultaneously through both inductors when the chopper operates with 220 V, the equivalent inductance, considering the mutual inductance and coupling coefficient near unity, is equal to four times $L_{\mathrm{r}1}$ or $L_{\mathrm{r}2}$, i.e., $L_{\mathrm{req}} = 4L_{\mathrm{r}1} = 4L_{\mathrm{r}2}$.

In Fig. 10, there are always two controlled semiconductors involved in the power transfer. Even though the input voltage is twice 110 V, the current through the semiconductors is reduced to half. Therefore, losses are approximately equal when the converter operates with 110 V.

V. Boost Converter

A classical boost converter shown in Fig. 12 is connected to the chopper. It is responsible for the output voltage regulation, PFC, and stepping the battery voltage up to the output voltage V_{bus}. In addition, this stage provides an active filtering to block the pulsating current of the nonlinear load (i.e., the inverter stage) from the battery bank. Switch S_b operates with zero-voltage switching in a wide range of output power using a passive nondissipative snubber circuit [16].

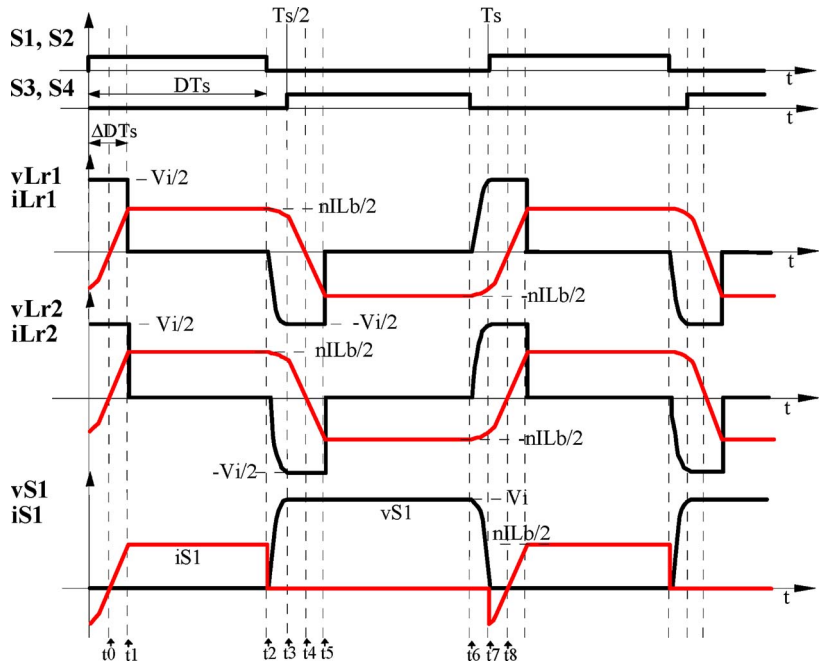

Fig. 11. Basic theoretical waveforms when the input voltage is 220 V.

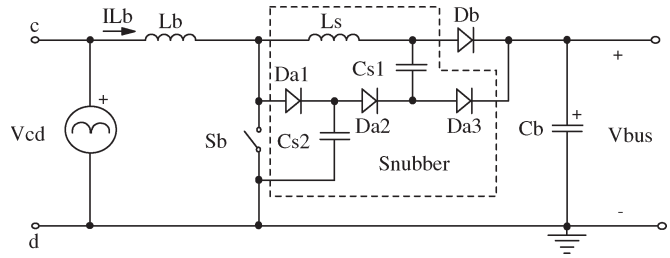

Fig. 12. Boost stage schematic.

The boost converter is controlled by using conventional average current mode control implemented with the well-known PWM IC UC3854B [13].

VI. Battery Charger

The battery charger is based on a small nonisolated buck converter, as shown in Fig. 13. The converter operates in continuous conduction mode of the current through the filter inductor and is supplied by the boost converter.

As the voltage across terminals c and d is chopped at 50 kHz and the ripple frequency is 120 Hz, as shown in Fig. 6, a controlled switch S_t is necessary. For this application, a thyristor associated with a passive snubber was used. Switch S_t is turned on when the ac mains voltage is null or out of the input voltage range, and it is turned off when the ac mains voltage is within the desired limits. The gating signal is turned off during normal operation; therefore, it is reverse biased naturally when $V_{\rm cd}$ voltage is higher than the battery bank voltage.

VII. Voltage-Source Inverter Stage

In order to perform dc–ac conversion, a classical voltage-source full-bridge inverter is connected to the output of the boost stage. The topology is shown in Fig. 14.

In order to control the output voltage, a sinusoidal PWM control with unipolar voltage switching was applied, synchronized with the utility. In order to protect the switches against overvoltages, a resistor-capacitor-diode (RCD) clamping snubber circuit was placed in each inverter leg, as shown in Fig. 14.

VIII. Simplified Design Example

A. Preliminary Specifications

The design specifications of the proposed UPS are shown in Table I. The switching frequency for all stages is assumed to be $f_{\rm s} = 50$ kHz.

The design parameters of the UPS stages are listed in Tables II–V.

B. Design Procedure of the Chopper Circuit

The rms output voltage of the chopper is calculated by using (8). Thus,

$$V_{\rm cd(rms)} = 1 \cdot \sqrt{2} \cdot 110 \cdot \sqrt{(0.48 - 0.048)} = 102.25 \text{ V}.$$

The peak output current of the chopper is determined using (9)

$$IL_{b(\rm pk)} \cong \frac{\sqrt{2} \cdot 1600}{102.25} \cong 19.36 \text{ A}.$$

The maximum duty-cycle reduction occurs when the voltage angle is $\theta = \pi/2$. Therefore, the inductance is obtained from (6) as

$$L_{\rm r1} = L_{\rm r2} = \frac{V_{i(\rm pk)_{110\,V}} \Delta D_{\max}}{2 f_{\rm s} n I L_{b(\rm pk)}}. \quad (10)$$

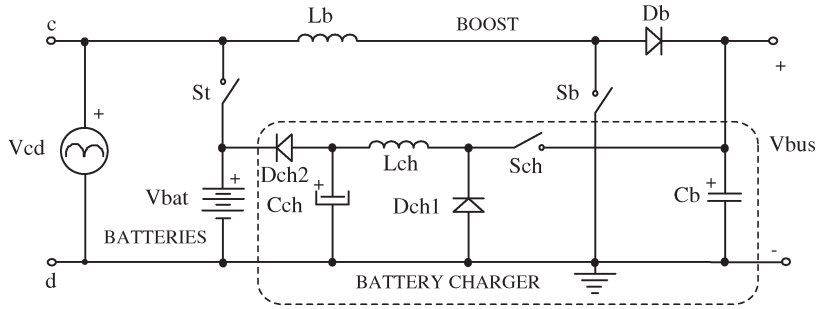

Fig. 13. Battery charger stage schematic.

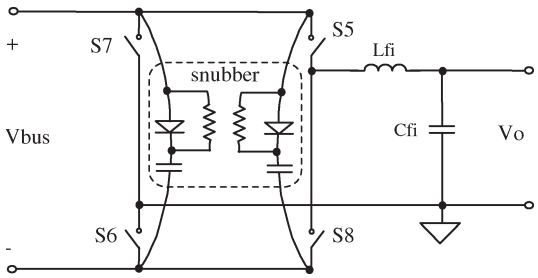

Fig. 14. Inverter stage schematic.

TABLE I
DEVELOPED UPS SPECIFICATIONS

Input voltage	V_i = 110Vac / 220Vac ±15%
Output voltage	V_o = 110Vac
Grid Frequency	f_r = 60Hz
Output Power Capacity	S_o = 2kVA
Output frequency	f_o = 60Hz
Input Power Factor	0.99
Output Power Factor	0.7
Number of Batteries (In series)	8 (12V/7Ah)

TABLE II
DESIGN PARAMETERS OF UPS CHOPPER STAGE

Transformer turns ratio	$n = N_p/N_s = 1$
Maximum duty cycle	$D_{\max} = 0.48$
Maximum duty cycle reduction	$\Delta D_{\max} = 0.048$

TABLE III
DESIGN PARAMETERS OF UPS BOOST STAGE

Boost inductor current ripple	$\Delta IL_{b\max} = 0.15 IL_{b(pk)}$
DC-link output voltage	V_{bus} = 220V
Hold-up time	$\Delta t = 8.333 \cdot 10^{-3}$s
Minimum DC link output voltage	V_1 = 190V

TABLE IV
DESIGN PARAMETERS OF UPS BATTERY CHARGER STAGE

Maximum battery voltage	V_{bat} = 108V
Maximum battery charge current	I_{ch} = 1A
Current ripple through the filter inductor	ΔI_{ch} = 0.1A
Duty cycle of the buck converter	D_{ch} = 0.49
Voltage ripple across battery bus	ΔV_{bat} = 0.2V

TABLE V
DESIGN PARAMETERS OF UPS INVERTER STAGE

Modulation index	ma = 0.71
Filter inductor ripple current	ΔIL_{fi} = 2.7A

Substituting the relevant parameters in (10), the inductances are given by

$$L_{\mathrm{r1}} = L_{\mathrm{r2}} = \frac{\sqrt{2} \cdot 110 \cdot 0.048}{2 \cdot 50\,000 \cdot 1 \cdot 19.36} = 3.85\ \mu\mathrm{H}.$$

The input filter capacitances must be small and arbitrarily chosen as $C_{\mathrm{f1}} = C_{\mathrm{f2}} = 6.6\ \mu$F, given for the connection of three paralleled polyester capacitors. The frequency of the chopper input current is twice the switching frequency. Thus, by using the LC filter criterion given in [18], i.e., $f_{\mathrm{f}} \leq 2f_{\mathrm{s}}/10$, the filter inductance is

$$L_{\mathrm{f}} = \frac{1}{C_{\mathrm{f(eq)}}(0.94 f_{\mathrm{s}})^2} \cong 137.18\ \mu\mathrm{H}. \tag{11}$$

C. Design Procedure of the Boost Converter

The boost inductance and filter capacitance are obtained according to Todd [13]

$$L_{\mathrm{b}} = \frac{\sqrt{2} V_{\mathrm{cd(rms)}} D_{\mathrm{boost}}}{f_{\mathrm{s}} \Delta I L_{b\max}} = 338.60\ \mu\mathrm{H} \tag{12}$$

$$C_{\mathrm{b}} = \frac{2 P_{\mathrm{o}} \Delta t}{V_{\mathrm{bus}}^2 - V_1^2} = 2167.9\ \mu\mathrm{F} \tag{13}$$

where

$$D_{\mathrm{boost}} = 1 - \frac{\sqrt{2} V_{\mathrm{cd(rms)}}}{V_{\mathrm{bus}}} = 0.34. \tag{14}$$

D. Design Procedure of the Battery Charger

The filter inductance is obtained by substituting the design parameters in the following equation:

$$L_{\mathrm{ch}} = \frac{V_{\mathrm{bat}}(1 - D_{\mathrm{ch}})}{f_{\mathrm{s}} \Delta I_{\mathrm{ch}}} = 11.01\ \mathrm{mH}. \tag{15}$$

TABLE VI
EXPERIMENTAL PARAMETERS OF UPS CHOPPER STAGE

Rectifier Diodes	GBPC3508A
Input Filter Inductor	L_f = 137.18μH
Input Filter Polyester Capacitors	$C_{f1} = C_{f2}$ = 3×2.2μF/400Vdc
Switches S_1–S_4	IXFX44N60
Coupled Inductors	$L_{r1} = L_{r2}$ = 3.9μH
High Frequency Transformer	NEE-65/39 (Thornton Ipec) Np=12 turns; Ns=12turns
Diodes D_{r1} and D_{r2}	HFA30PA60C

The filter capacitance and equivalent series resistance are calculated, respectively, as

$$C_{\rm ch} = \frac{\Delta I_{\rm ch}}{8 f_{\rm s} \Delta V_{\rm bat}} = 1.25\ \mu{\rm F} \tag{16}$$

$$R_{\rm se} \leq \frac{\Delta V_{\rm bat}}{\Delta I_{\rm ch}} \leq 2\ \Omega. \tag{17}$$

The prototype was implemented by using an electrolytic capacitor rated at 100 μF/250 V.

E. Design Procedure of the Voltage-Source Inverter

The filter inductance is obtained from the inductor voltage equation, which is similar to (1). The design considers purely resistive load, and the angle of the fundamental input voltage across the LC filter is $\theta = \omega t = \pi/2$. Substituting the design parameters in (18) gives

$$L_{\rm fi} \cong \frac{\left(V_{\rm bus} - \sqrt{2} V_{\rm o}\right) ma}{2 f_{\rm s} \Delta I L_{\rm fi}} = 170\ \mu{\rm H}. \tag{18}$$

The resonance frequency of the output LC filter applying a unipolar voltage switching technique is given by [18]

$$f_{\rm fi} \leq \frac{2 f_{\rm s}}{10} = \frac{1}{2\pi \sqrt{L_{\rm fi} C_{\rm fi}}}. \tag{19}$$

The inverter output filter capacitance must be greater than $C_{\rm fi} \geq 1.49\ \mu$F. The prototype was implemented with a metalized polypropylene capacitor rated at 30 μF/250 V.

IX. EXPERIMENTAL RESULTS

In order to verify the feasibility and performance of the proposed UPS, which was assembled with the parameters obtained in Section VIII (shown in Tables VI–IX), a laboratory prototype was implemented and evaluated.

A photograph of the developed prototype is shown in Fig. 15, where the power conversion stages, magnetics components, and the battery bank can be seen.

The experimental results consist of relevant voltage and current waveforms and also efficiency and power factor curves.

TABLE VII
EXPERIMENTAL PARAMETERS OF UPS BOOST STAGE

Boost Inductor	L_b = 338.60μH
Output Electrolytic Capacitors	C_b = 3×680μF/450V
Diode D_b	HFA25PB60
Switch S_b	IXFX44N60
Resonant Inductors	L_S = 0.9μH
Polypropylene Film Capacitors	C_{S1} = 120nF C_{S2} = 6.8nF
Diodes D_{a1}, D_{a2} and D_{a3}	MUR460
Static Switch (S_t)	40TPS12

TABLE VIII
EXPERIMENTAL PARAMETERS OF UPS BATTERY CHARGER STAGE

Filter Inductor	L_{ch} = 11mH
Output Electrolytic Capacitor	C_{ch} = 100μF/250V
Switch S_{ch}	IRF740
Diodes D_{ch1} and D_{ch2}	MUR460

TABLE IX
EXPERIMENTAL PARAMETERS OF UPS INVERTER STAGE

Output Filter Inductor	L_{fi} = 170μH
Output Filter Polyprop. Capacitor	C_{fi} = 30μF
Switches S_5 - S_8	IXFX44N60

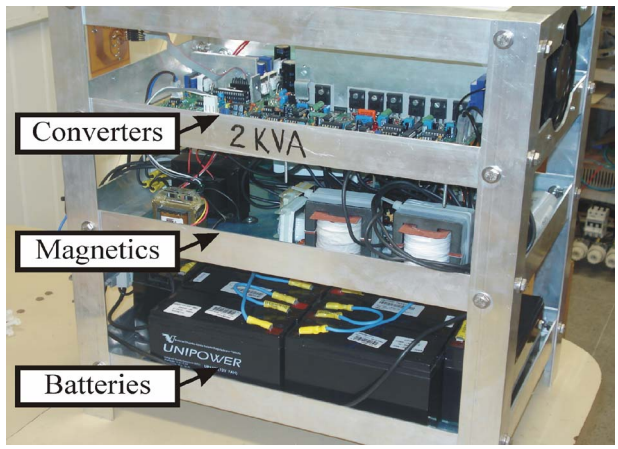

Fig. 15. UPS laboratory prototype.

A. Waveforms and Curves for the Grid-Mode Operation

The grid-mode-operation experimental results were realized for two different input voltage levels. The results shown in Figs. 16–19 were obtained for an input voltage equal to 110 $V_{\rm ac}$, and the results shown in Figs. 20–23 were obtained for an input voltage equal to 220 $V_{\rm ac}$. The nonlinear load used for the tests complies with the requirements of IEC62040-3 [19].

Fig. 16 shows the input voltage and input current waveforms. It can be observed from the figure that the input current waveform is close to sinusoidal and has a unity input power factor. Fig. 17 shows the voltage and the current waveforms regarding switch S_1, where soft commutation details can be seen. The output voltages and currents of the inverter are shown

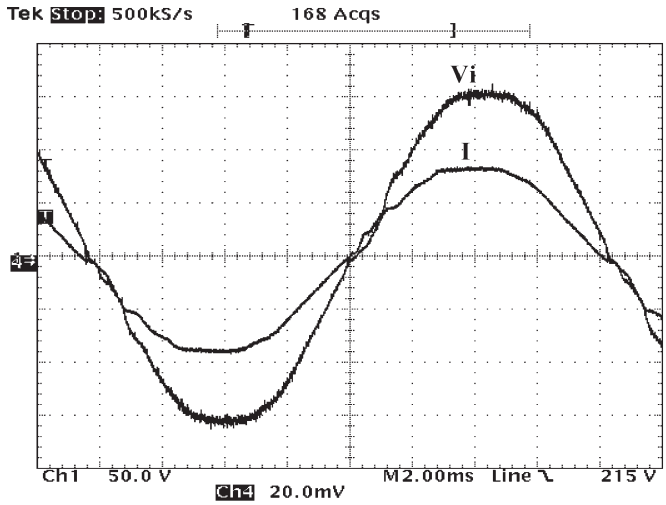

Fig. 16. Mains input voltage and current (Ch1: 50 V/div; Ch4: 10 A/div; 2 ms/div).

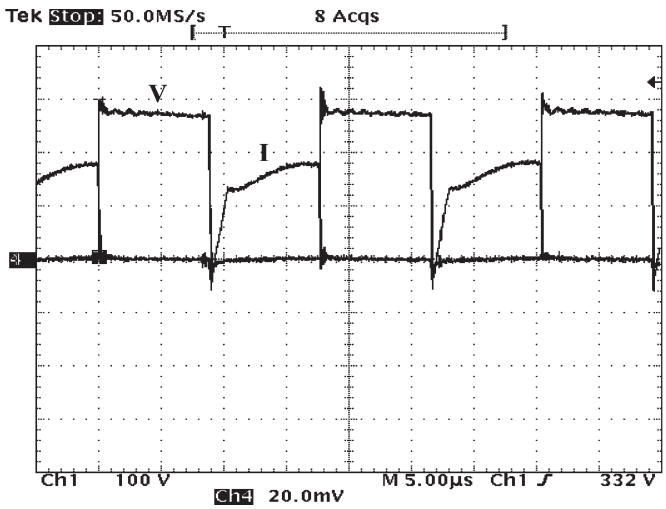

Fig. 17. Voltage and current of the chopper switch S_1 (Ch1: 100 V/div; Ch4: 10 A/div; 5 μs/div).

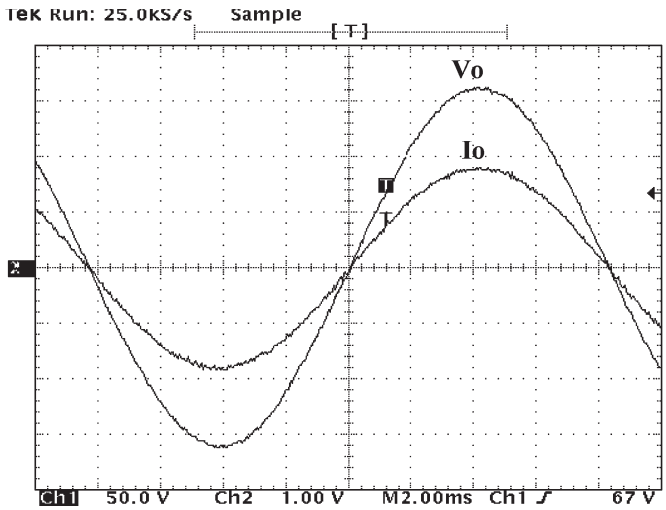

Fig. 18. Output voltage and current of the inverter for linear load (Ch1: 50 V/div; Ch2: 10 A/div; 2 ms/div).

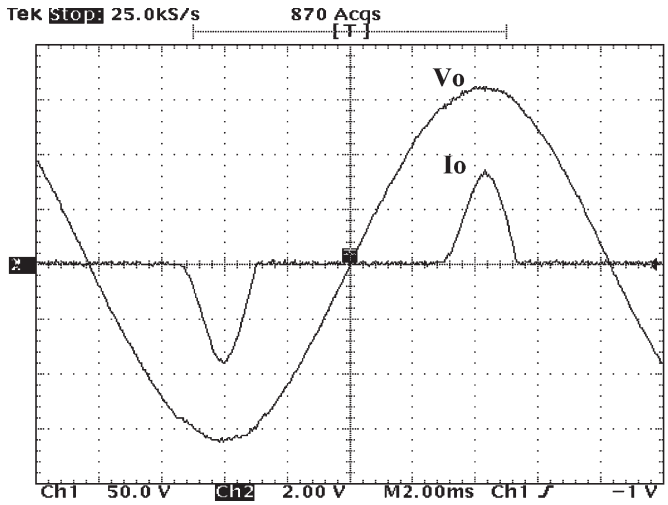

Fig. 19. Output voltage and current of the inverter for nonlinear load (Ch1: 50 V/div; Ch2: 20 A/div; 2 ms/div).

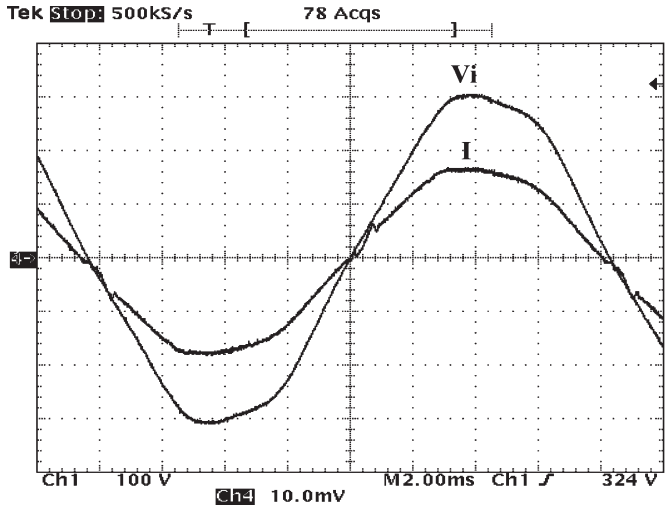

Fig. 20. Mains input voltage and current (Ch1: 100 V/div; Ch4: 5 A/div; 2 ms/div).

in Figs. 18 and 19, where a high-quality sinusoidal voltage waveform is obtained, independently of the load characteristic. The analysis of the waveforms for an input voltage equal to 220 V_{ac} (shown in Figs. 20–23) is similar to the case when the input voltage is 110 V_{ac}.

The utility input voltage and current, battery current, as well as the output voltage waveform for full-load operation, and an input voltage equal to 220 V_{ac} are shown in Fig. 24, when the UPS transition from grid mode to battery mode occurs. Notice that the load voltage continues to regulate despite the ac main failures. When the utility voltage is finally restored, the load voltage behavior is almost the same, as shown in Fig. 25.

The UPS efficiency and power factor versus output power for linear load characteristic are shown in Figs. 26 and 27, respectively, where the indicated voltage (110 V or 220 V) refers to the input voltage levels. According to the experimental results for the grid mode, the proposed UPS achieved a high efficiency despite the higher switching frequency of

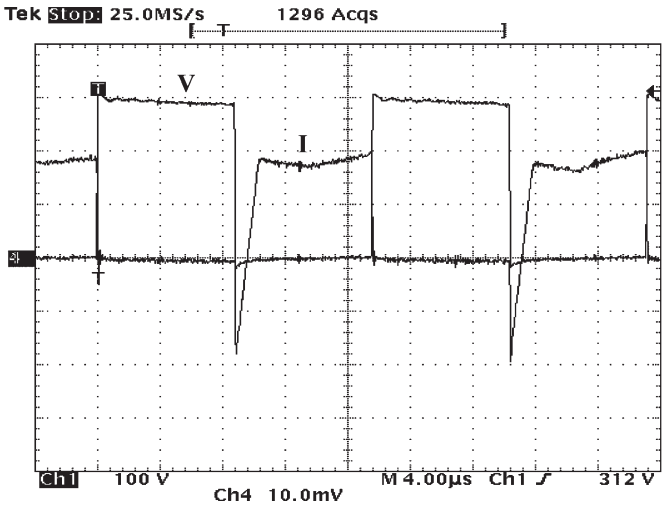

Fig. 21. Voltage and current of the chopper switch S_1 (Ch1: 100 V/div; Ch4: 5 A/div; 4 μs/div).

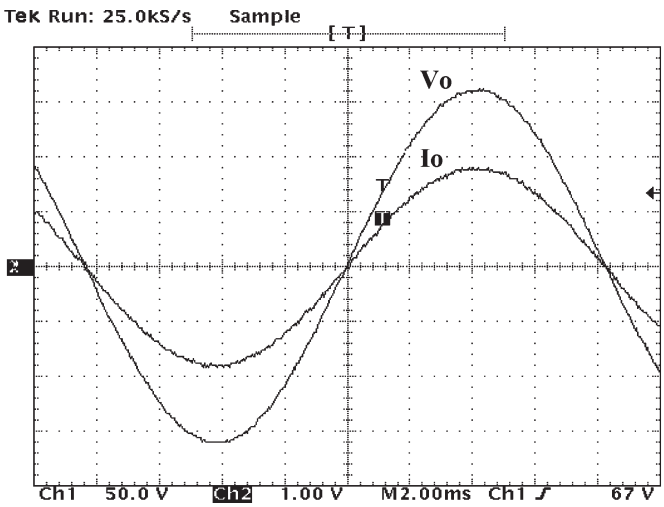

Fig. 22. Output voltage and current of the invert for linear load (Ch1: 50 V/div; Ch2: 10 A/div; 2 ms/div).

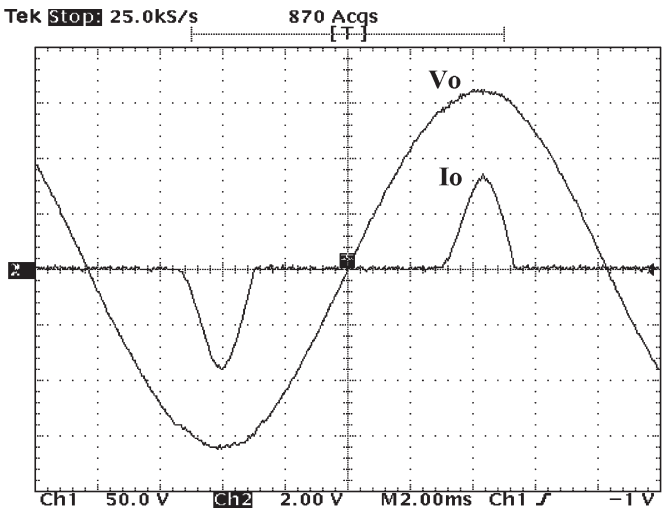

Fig. 23. Output voltage and current of the inverter for nonlinear load (Ch1: 50 V/div; Ch2: 20 A/div; 2 ms/div).

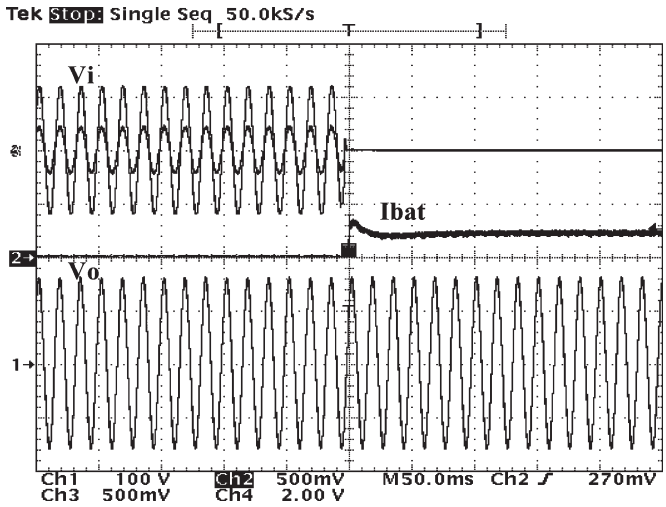

Fig. 24. UPS transition from grid-mode to battery-mode operation. From top to bottom: Input voltage and current, battery current, and output voltage (Ch1: 100 V/div; Ch2: 25 A/div; Ch3: 250 V/div; Ch4: 20 A/div; 50 ms/div).

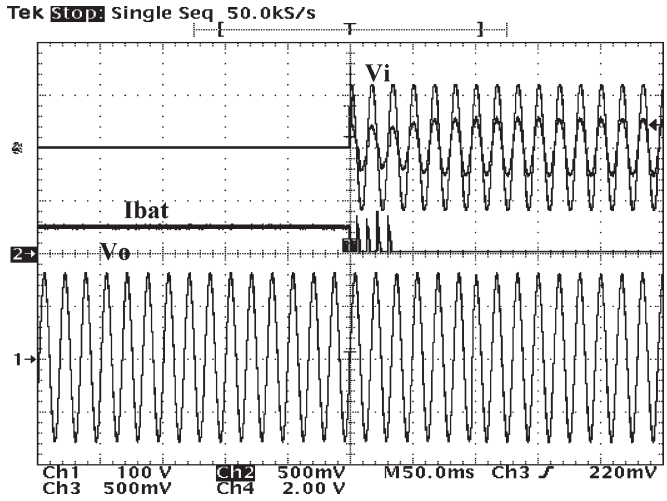

Fig. 25. UPS transition from battery-mode to grid-mode operation. From top to bottom: Input voltage and current, battery current, and output voltage (Ch1: 100 V/div; Ch2: 25 A/div; Ch3: 250 V/div; Ch4: 20 A/div; 50 ms/div).

the controlled switches and the amount of power processing stages.

B. Waveforms for the Battery-Mode Operation

The experimental results for the battery-powered mode were carried out only for the nonlinear load connected at the output. The battery set voltage was adjusted around 100 V, which represents the rated voltage during normal test conditions.

The characteristics of the nonlinear load were the same as used in grid-mode operation. Fig. 28 shows the voltage and current in the battery bank as well as the output voltage of the inverter. As shown in Fig. 28, by using the average current mode control, a continuous dc current with a low ripple has been drawn from the battery set, blocking the pulsed current

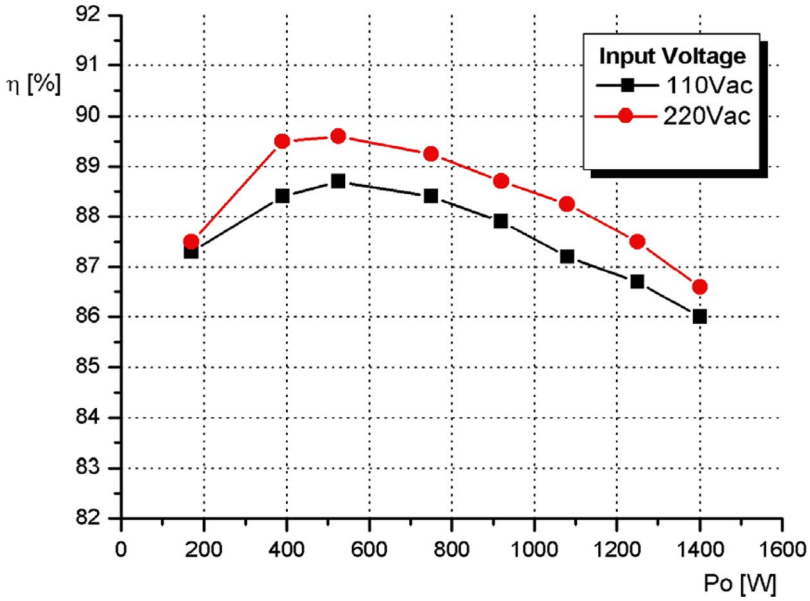

Fig. 26. Efficiency of the UPS in grid-mode operation as a function of the output power.

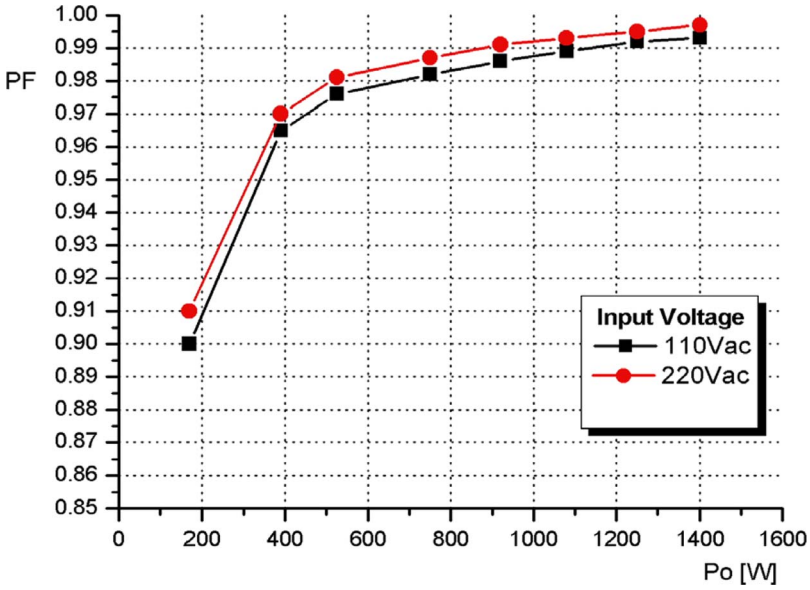

Fig. 27. Input power factor behavior of the UPS in grid-mode operation as a function of the output power.

required by the inverter operation, thus enhancing the reliability and life of the battery set.

X. Conclusion

This paper has proposed a feasible double-conversion UPS that uses high-frequency transformer isolation, which is suitable to operate with rms input voltages equal to 110–220 V, 115–230 V, or 120–240 V. The qualitative analysis for the input voltage equal to 110–220 V, a simple design example, and experimental results obtained from a 2-kVA prototype have been presented.

As shown in Figs. 16 and 20, the system presents PFC. This characteristic is due to the boost stage, which is controlled using the well-known average current mode control. The maximum input power factor obtained at full load is near unity, as shown in Fig. 27, when the UPS was fed with 220 V_{ac}.

The chopper stage converts the continuous input voltage to high-frequency ac voltage, so that the use of a high-frequency transformer is possible. The chopper switches present soft commutation, as shown in Figs. 17 and 21. Therefore, commutation losses are reduced.

The inverter stage presents a sinusoidal output voltage when supplying linear or nonlinear loads, as shown in Figs. 18, 19, 22, 23, and 28. Hard commutation of the switches is verified; therefore, in order to limit the voltage overshoot across them, a simple RCD snubber was used.

Finally, the experimental results demonstrated the effectiveness and soundness of the proposed UPS. The global efficiency obtained at full load for grid-mode operation was 86% for an

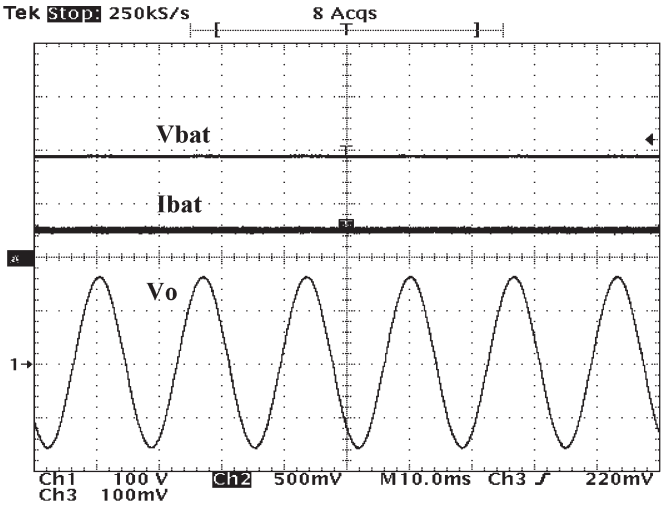

Fig. 28. UPS operation during battery mode. From top to bottom: Battery voltage and current, and the output voltage (Ch1: 100 V/div; Ch2: 25 A/div; Ch3: 50 V/div; 10 ms/div).

input voltage equal to 110 V and 86.5% for an input voltage equal to 220 V, as shown in Fig. 26.

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