A Three-Phase ZVS PWM DC–DC Converter Associated With a Double-Wye Connected Rectifier, Delta Primary

Demercil S. Oliveira Jr., Fernando L. M. Antunes, *Member, IEEE*, and Carlos E. A. Silva

***Abstract*—This paper presents the theoretical analysis of the three-phase zero voltage switching pulsewidth modulation dc–dc converter associated with a double Wye connected rectifier, delta primary, using a special switching scheme in order to maintain equilibrium among the currents through the output filters. The operating stages are described and the simulation and experimental results of a 6-kW prototype are presented.**

***Index Terms*—DC–DC converter, three-phase, zero voltage switching (ZVS) commutation.**

I. Introduction

THE main topology used in high power dc–dc conversion is the zero voltage switching (ZVS) pulsewidth modulation (PWM) full bridge converter with phase-shift control [1], [2]. However, at higher power levels, the components face several stresses. An interesting alternative was proposed by Ziogas [3]. It uses a three-phase inverter coupled to a three-phase high frequency transformer and to a three-phase high frequency rectifier. The resulting advantages consist of the increase of the input and output current frequency by a factor of three compared to the full-bridge converter, lower rms current through power components, and reduction of the cores. Although it presents satisfactory advantages, soft commutation has not been achieved, which limits the switching frequency and the power density.

Divan [4] has proposed a circuit in which soft commutation can be achieved for a wide load range. Nevertheless, it is only viable in applications where bidirectional power flow is needed, because six additional switches are included. Bhat [5] and Ziogas [6] applied the resonance concept in three phase dc–dc converters, reaching soft commutation. However, the resulting topologies suffer high voltage and current stresses, and also a considerable increase in the volume of reactive power elements.

Then, the use of asymmetrical duty cycle [7] in the three-phase dc–dc converter was proposed in [8], in order to provide ZVS commutation of all switches for a wide load range, as shown in Fig. 1.

Manuscript received August 25, 2005; revised February 21, 2006. This work was supported in part by CNPq. Recommended by Associate Editor A. von Jouanne.

D. S. Oliveira, Jr. is with the Power Processing and Control Group, Energy Processing and Control Group, Federal University of Ceará, Ceará BR-60431970, Brazil (e-mail: demercil@dee.ufc.br).

F. L. M. Antunes and C. E. A. Silva are with the Energy Processing and Control Group, Federal University of Ceará, Ceará BR-60431970, Brazil.

Digital Object Identifier 10.1109/TPEL.2006.882937

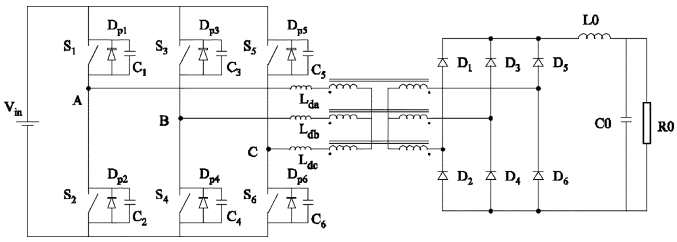

Fig. 1. Association with the three-phase full-bridge rectifier [8].

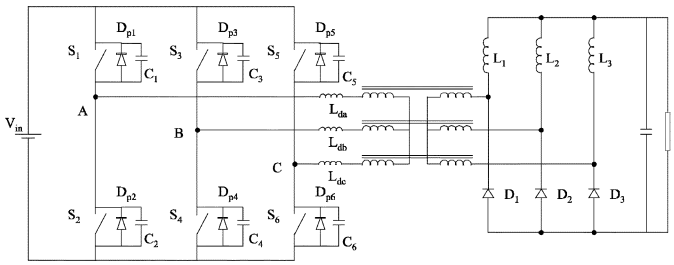

Fig. 2. Association with the hybridge rectifier [9], [10].

Nevertheless, analogously to the full-bridge converter, the resulting topology suffers higher conduction losses in the rectifier stage, since two series diodes conduct the load current. Therefore, the association of a three-phase dc–dc converter and a three-phase high efficiency rectifier seems to be an optimal arrangement for applications that demand high current levels and low output voltages. In [9] and [10] (see Fig. 2), the use of a three-phase version of the hybridge rectifier improved efficiency in about 2%. However, there is a natural increase in the output inductors volume. Besides, disequilibrium among the currents through the output inductors causes the output inductors to be over designed, implying even more increased volume. In [11], the use of a zig-zag connection in the output filters is proposed in order to mitigate disequilibrium, but at cost of increased volume. Within this context this paper introduces the use of the double-Wye connected rectifier with the interphase inductors acting as output inductor filter.

II. Proposed Three-Phase Rectifier

A. Proposed Topology

In order to overcome the efficiency limit imposed by the full-bridge rectifier used in [8], without causing the increase of the output inductors [10], this paper proposes the use of double-Wye connection in the transformer [12]. This rectifier is formed by six diodes $(D_1, D_2, \ldots, D_6)$ and two output inductors L_{01} and

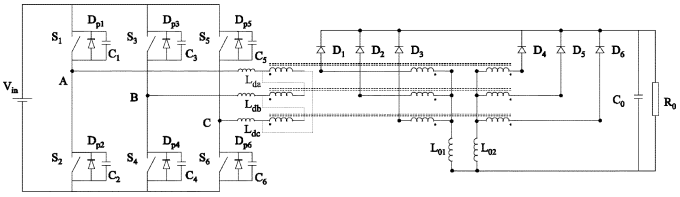

Fig. 3. Three-phase ZVS dc–dc converter associated with the hybridge rectifier.

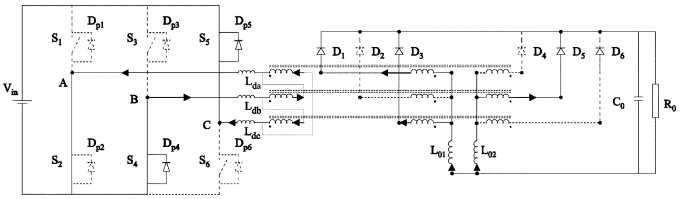

Fig. 4. First stage in Region 1.

TABLE I
OPERATING STAGES OF REGION 1

	First Stage	Second Stage	Third Stage	Fourth Stage
$i_{Ldc}(t)$	$-\frac{I_L}{2}-\frac{1}{3}\frac{V_{in}}{L_d}t$	$-I_L+\frac{1}{6}\frac{V_{in}}{L_d}t$	$-\frac{I_L}{2}$	$-\frac{I_L}{2}$
$i_{Ldb}(t)$	$I_L-\frac{1}{3}\frac{V_{in}}{L_d}t$	$\frac{I_L}{2}-\frac{1}{3}\frac{V_{in}}{L_d}t$	$-\frac{I_L}{2}$	$-\frac{I_L}{2}$
$i_{Lda}(t)$	$-\frac{I_L}{2}+\frac{2}{3}\frac{V_{in}}{L_d}t$	$\frac{I_L}{2}+\frac{1}{6}\frac{V_{in}}{L_d}t$	I_L	I_L
$i_{Lpa}(t)$	I_f	$-I_f+\frac{1}{6}\frac{V_{in}}{L_d}t$	0	0
$i_{Lpb}(t)$	$I_f-\frac{1}{3}\frac{V_{in}}{L_d}t$	$-\frac{1}{6}\frac{V_{in}}{L_d}t$	$-I_f$	$-I_f$
$i_{Lpc}(t)$	$\frac{1}{3}\frac{V_{in}}{L_d}t$	I_f	I_f	I_f
Δt	$\frac{3L_d}{V_{in}}I_f$	$\frac{6L_d}{V_{in}}I_f$	$DT_s-\Delta t_1-\Delta t_2$	$(1-D)T_s$
V_{f1}	0	V_{in}	V_{in}	0
V_{f2}	0	$\frac{V_{in}}{2}$	V_{in}	0

L_{02}, as shown in Fig. 3. The output inductors act as an interphase inductor as well as an output filter. The use of two inductors does not increase volume if compared to the full-bridge rectifier.

B. Operating Stages

The sequences regarding the operating stages depend on the duty cycle and the input peak current. There are three possible distinct sequences that are defined as Regions 1, 2, and 3, as it can be seen clearly in the static gain curve of the converter (Fig. 21).

The line currents are defined by $i_{Lda}, i_{Ldb}, i_{Ldc}$, the phase currents are $i_{Lpa}, i_{Lpb}, i_{Lpc}$ and the voltages across the output filters are given by V_{f1} and V_{f2}, according to Fig. 3. Time intervals for stage i are designated by Δt_i. Besides, duty cycle D is applied to switches S_1, S_3, and S_5 and D' is equal to $(1-D)$. The gating signals for switches $S_1, S_2, \ldots, S_6$ are defined by V_{g1}, V_{g2}, and V_{g6}. The operating stages are described considering ideal transformer and semiconductors.

Region I: The expressions representing line and phase currents, voltages applied to the output filters, and time intervals of each operating stage for Region 1 are presented in Table I.

First Stage $[t_0, t_1]$*:* This stage begins when switch S_5 is turned on (Fig. 4). All line and phase currents have linear behavior, according to Fig. 8. At the end of this stage, diode D_3 is reverse biased and diode D_6 is forward biased.

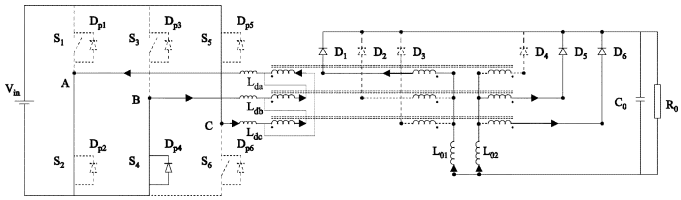

Fig. 5. Second stage in Region 1.

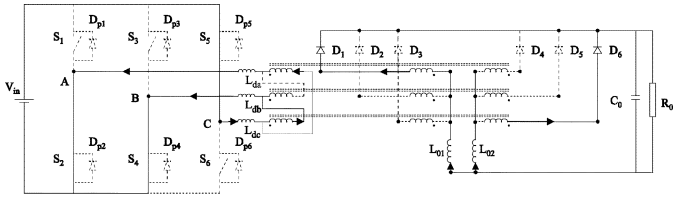

Fig. 6. Third stage in Region 1.

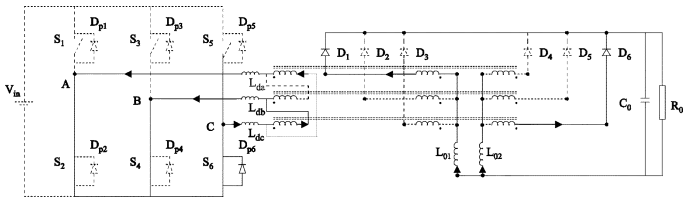

Fig. 7. Fourth stage in Region 1.

Second Stage $[t_1, t_2]$*:* As i_{Lpa} reaches its maximum value, i_{Lpb} and i_{Lpc} vary linearly, causing the linear transition in the line currents, as in Fig. 8. At the end of this stage, diode D_5 is reverse biased and diode D_6 conducts i_{L02} (Fig. 5). This additional transition stage is responsible for disequilibrium between output currents i_{L01} and i_{L02}.

Third Stage $[t_2, t_3]$*:* When the linear transitions finish, energy transference begins, until switch S_5 is turned off (Fig. 6).

Fourth Stage $[t_3, t_4]$*:* This stage begins when the PWM controller determines the end of the duty cycle (Fig. 7). The behavior of the circuit is shown in Fig. 8, representing a freewheeling stage.

From the aforementioned analysis, one can obtain the average voltage applied to each output filter in Region 1 $(R=1)$ as

$$V_{f1+}^{R=1} = V_{\text{in}}\left[3D - 4.5\frac{L_d}{V_{\text{in}}T_s}I_L\right] \quad (1)$$

$$V_{f2+}^{R=1} = V_{\text{in}}\left[3D - 9\frac{L_d}{V_{\text{in}}T_s}I_L\right] \quad (2)$$

where I_L is the peak value of the line currents (or the peak value of the input current).

The difference between the average voltages, verified in the second stage, causes disequilibrium in the currents through inductors L_{01} and L_{02}. Then, according to [13], conventional switching schemes can not provide output voltage control of this converter [14].

Region II: Region 2 occurs when duty cycle is slightly greater than 0.33, i.e., when turning off occurs before the end of a linear stage, as shown in Fig. 13.

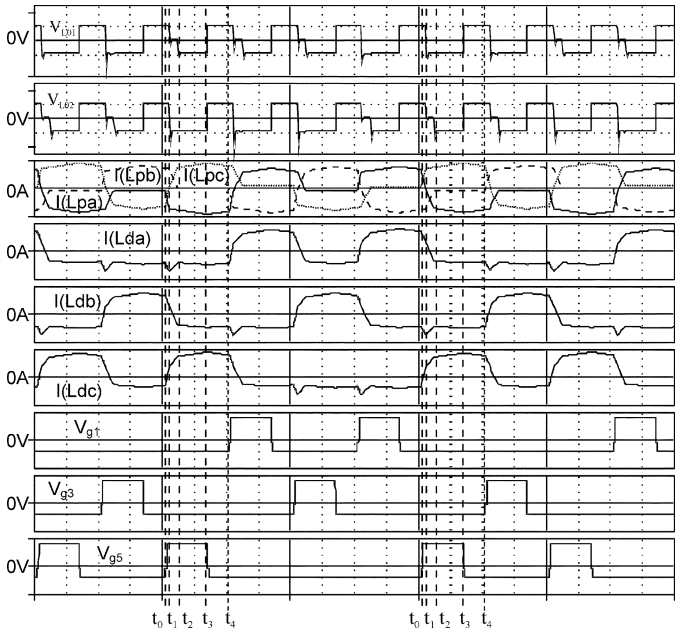

Fig. 8. Main waveforms in Region 1.

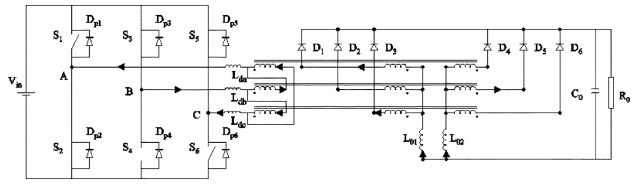

Fig. 9. First stage in Region 2.

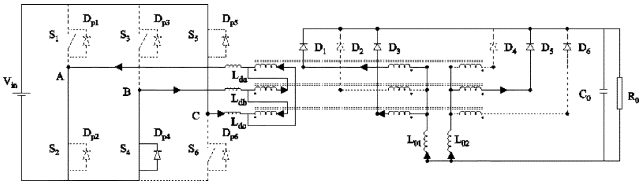

Fig. 10. Second stage in Region 2.-6pt

First Stage $[t_0, t_1]$*:* This stage begins when switch S_5 is turned on (Fig. 9). All line and phase currents have linear behavior. The time interval for this stage is defined by the difference between the duty cycle and 0.33.

Second Stage $[t_1, t_2]$*:* Switch S_3 is turned on at instant t_2 (Fig. 10). The currents present a linear transition until i_{Lpa} reaches its minimum value. There is no energy transference during this stage.

Third Stage $[t_2, t_3]$*:* Partial energy transference begins, until the end of the linear transitions of line currents (Fig. 11).

Fourth Stage $[t_3, t_4]$*:* When all linear transitions finish, there is full energy transference, what occurs until the next switching cycle (Fig. 12).

From the aforementioned analysis, one can obtain the average voltage applied to each output filter in Region 2 $(R = 2)$ as

$$V_{f1+}^{R=2} = V_{\text{in}} \left[1 - 4.5 \frac{L_d}{V_{\text{in}} T_s} I_L \right] \tag{3}$$

$$V_{f2+}^{R=2} = V_{\text{in}} \left[\frac{3}{2} D + \frac{1}{2} - 9 \frac{L_d}{V_{\text{in}} T_s} I_L \right] \tag{4}$$

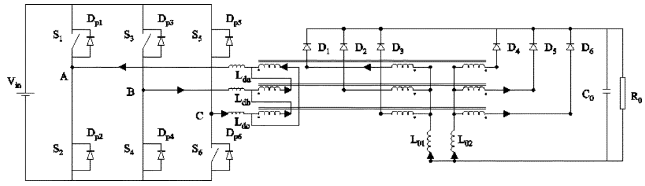

Fig. 11. Third stage in Region 2.

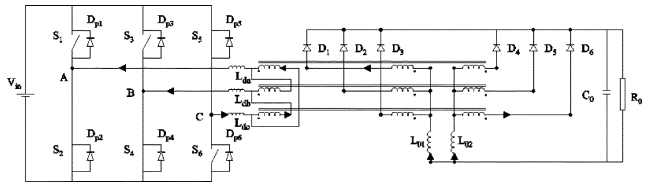

Fig. 12. Fourth stage in Region 2.

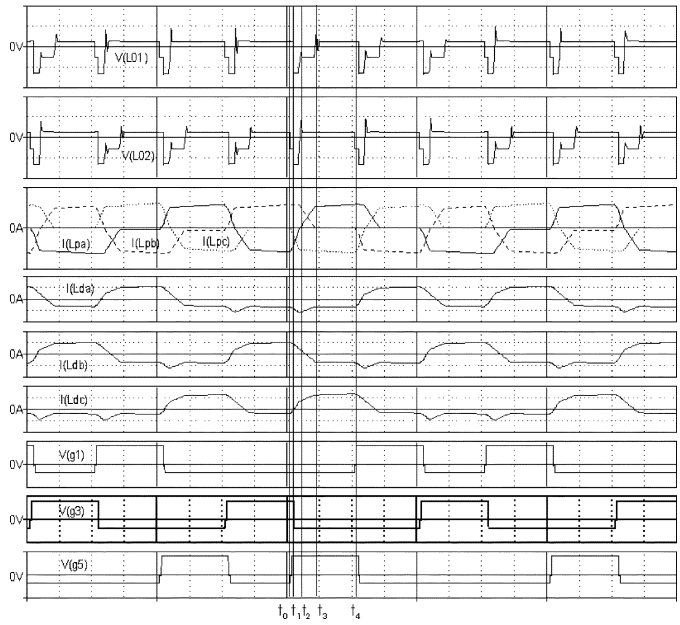

Fig. 13. Main waveforms for Region 2.

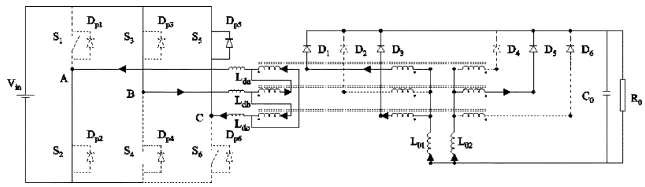

Fig. 14. First stage in Region 3.

where I_L is the peak value of the line currents (or the peak value of the input current).

Region III: Region 3 occurs when duty cycle is near 0.5, and is characterized by a constant and maximum static gain.

First Stage $[t_0, t_1]$*:* This stage begins when switch S_5 is turned on (Fig. 14). All line and phase currents have linear behavior, according to Fig. 18. There is full energy transference through L_{02} and partial energy transference through L_{01}.

Second Stage $[t_1, t_2]$*:* When the linear transitions finish, the second stage and full energy transference begin (Fig. 15). All line currents remain constant.

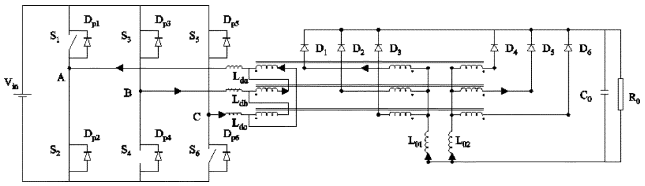

Fig. 15. Second stage in Region 3.

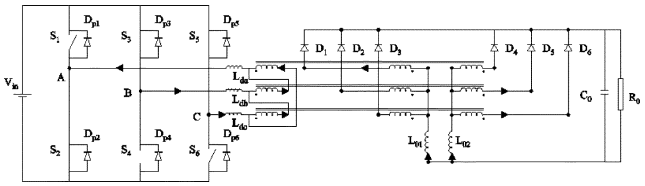

Fig. 16. Third stage in Region 3.

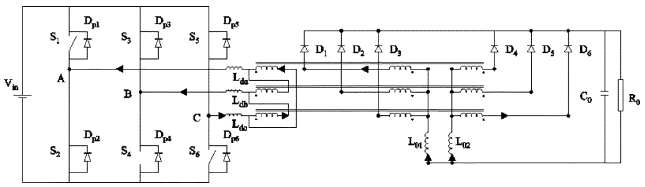

Fig. 17. Fourth stage in Region 3.

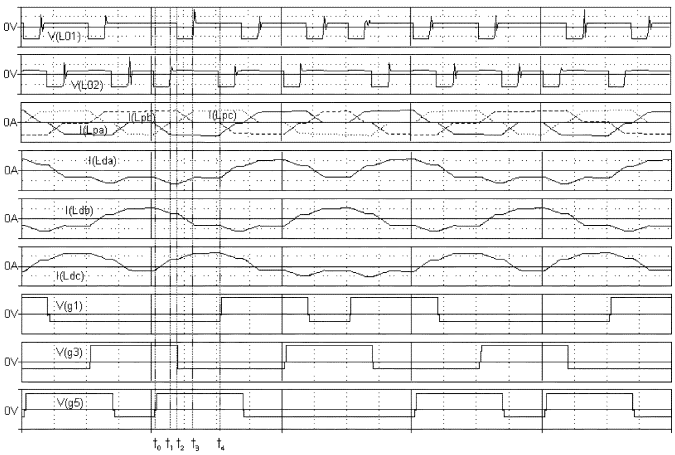

Fig. 18. Main waveforms for Region 3.

Third Stage $[t_2, t_3]$*:* This stage is similar to the first one, but full energy transference occurs through L_{02} instead (Fig. 16).

Fourth Stage $[t_3, t_4]$*:* As in the second stage, it begins when the linear transitions of the previous stage finish (Fig. 17).

From the aforementioned analysis, one can obtain the average voltage applied to each output filter in Region 3 $(R = 3)$ as

$$V_{f1+}^{R=3} = V_{f2+}^{R=3} = V_{\text{in}}\left[1 - 4.5\frac{L_d}{V_{\text{in}}T_s}I_L\right] \tag{5}$$

where I_L is the peak value of the line currents (or the peak value of the input current).

C. PN Modulation

From (1)–(4), one can see a average voltage difference between the voltages applied to each output filter. Then, there is a natural disequilibrium between the output inductors currents. A new switching scheme is then proposed in order to mitigate the average voltage difference between the output filters.

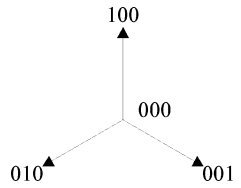

Fig. 19. Vectors in each operating mode.

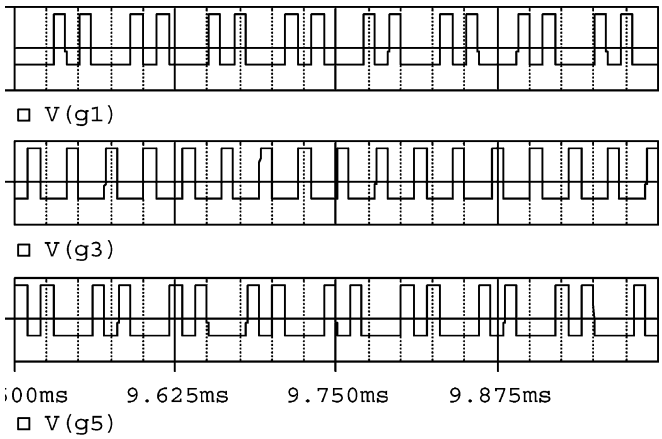

Fig. 20. Gating signals for D =0.33.

According to the aforementioned analysis, for D <0.33 (Region 1), the possible vectors are shown in Fig. 19, where "1" and "0" correspond to the ON and OFF states of switch S_i, respectively. The expressions in Table I are obtained using clockwise sequence (100−000−010−000−001), that is represented by the sign "+." However, for anticlockwise sequence, that is represented by the sign "−," $V_{f1-} = V_{\text{in}}/2$ and $V_{f2-} = V_{\text{in}}$, in the second stage (see Fig. 20). As a result, the average voltages applied to each output filter, for anticlockwise sequence, are given by

$$V_{f1-}^{R=1} = V_{\text{in}}\left[D' - 9\frac{L_d}{V_{\text{in}}T_s}I_L\right] = V_{f2+}^{R=1} \tag{6}$$

$$V_{f2-}^{R=1} = V_{\text{in}}\left[D' - 4.5\frac{L_d}{V_{\text{in}}T_s}I_L\right] = V_{f1+}^{R=1}. \tag{7}$$

Then, a new switching scheme, named "PN Modulation" is proposed, which consists of the use of clockwise and anticlockwise sequences in an alternate way (100−010−001−100−001−010). Therefore, the average voltage applied to each output filter for two switching periods became equal and are given by (8), as the disequilibrium between the currents through the output inductors is minimized, enabling output voltage control with pulse width modulation

$$V_0^{R=1} = V_{f1}^{R=1} = V_{f2}^{R=1} = V_{\text{in}}\left[D' - 6.75\frac{L_d}{V_{\text{in}}T_s}I_f\right]. \tag{8}$$

D. Static Gain

From the theoretical analysis shown in Table I and expression (8), one can obtain the static gain curve represented in Fig. 21, which corresponds to the operating modes (Regions 1, 2, and 3). However, operation in Region 3 must be avoided if output voltage regulation is required.

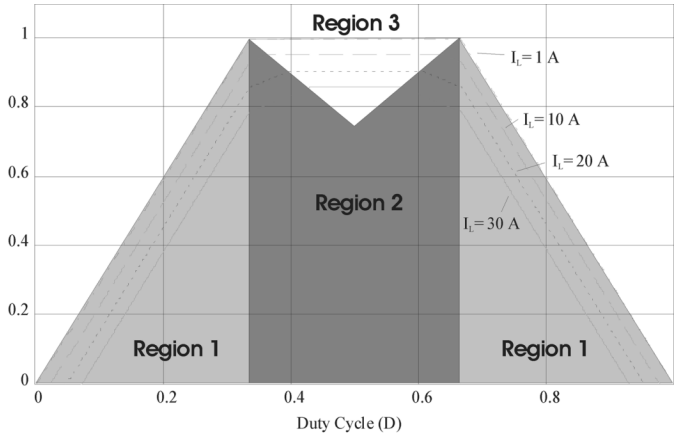

Fig. 21. Static gain.

E. Unbalance Considerations

Disequilibrium between the currents through the output inductors causes dc unbalance and consequently core saturation, if three uncoupled transformers are used. Therefore an optimum equilibrium is a must, as obtained in the PN modulation.

In a secondary double-Wye connection without interphase inductors, there is ac unbalance, which is not acceptable, since it promotes an ac flux path outside of the core. The presence of interphase inductors mitigates such unbalance and reduces rms currents through the secondary windings, as well as through output diodes $D_1, D_2, \ldots, D_6$, because it increases the conduction angle.

F. Volume Analysis

In this section, a comparison between the volumes of output inductors in the proposed rectifier and in the hybridge rectifier will be presented. The same specifications for the design of both converters are assumed.

From the equations developed above, inductances L_{01} and L_{02} can be obtained by

$$L_0 > \frac{V_{\text{in}}}{12 n f_s \Delta I_L} \tag{9}$$

and the energy stored in each inductor is given by

$$E_{yy} = \frac{1}{2} L_{01} I_{01}^2 = \frac{1}{2} L_{02} I_{02}^2 = \frac{V_{\text{in}}}{12 n f_s \Delta I_L} \left(\frac{I_0}{2} + \frac{\Delta I_L}{2} \right)^2. \tag{10}$$

Then, the ratio between the amounts of energy stored in the inductors using the proposed rectifier and the hybridge one is given by

$$\frac{E_{yy}}{E_{\text{hy}}} = 3 \frac{n_{\text{hy}}}{n_{yy}} \frac{\Delta I_{Lhy}}{\Delta I_{Lyy}} \frac{(I_0 + \Delta I_{Lyy})^2}{(2I_0 + 3\Delta I_{Lhy})^2}. \tag{11}$$

Assuming an accurate transformer design, the relationship between the transformer ratio n_{yy} in the proposed rectifier and the transformer ratio n_{hy} in the hybridge rectifier is given by

$$\frac{n_{\text{hy}}}{n_{yy}} = 1,5. \tag{12}$$

TABLE II
VOLUME COMPARISON (NORMALIZED QUANTITIES)

Inductor ANALYSIS					
	Energy	A_p	**Volume**	**Number of Inductors**	**Total Volume**
Proposed Rectifier (YY)	0.75	0.72	0.8	2	1,6
Hybridge Rectifier (HY)	1	1	1	3	3
TRANSFORMER ANALYSIS					
	Power Handling	A_p	**Volume**	**Number of Transformers**	**Total Volume**
Proposed Rectifier (YY)	1.21	1.24	1.16	3	3.47
Hybridge Rectifier (HY)	1	1	1	3	3

TABLE III
MAIN SPECIFICATIONS

V_{IN}	V_0	P_0	F_S
420V	60V	6kW	46kHz

TABLE IV
COMPONENTS DESCRIPTION

S_1, S_2, S_3, S_4, S_5, S_6	IRG4PC50UD	L_{da}=L_{db}=L_{dc}	EE42/21/15 – 4400 – IP12 N = 12
D_1, D_2, D_3, D_4, D_5, D_6	HFA30PA60C	L_{01}=L_{02}	2xEE55/28/21 – IP12 N = 7
Transformer	EE65/33/39 – 10800 – IP12 N_p=20 N_s=4	C_0	4x470µF/100V

Also, in order to maintain the same current ripple in the switches of both converters, the current ripple is assumed as ten percent of the inductor current

$$\Delta I_{Lhy} = 0.1 \frac{I_0}{3} \tag{13}$$

$$\Delta I_{Lyy} = 0.1 \frac{I_0}{2}. \tag{14}$$

Substituting (12)–(14) in (11), the following energy ratio for one inductor is obtained:

$$\frac{E_{yy}}{E_{\text{hy}}} = 0.75. \tag{15}$$

From the developed equations and considering that the inductor volume is given by $5.7 A_p^{0.68}$, Table II was obtained. It can be seen that the total output inductor volume is almost half of that in the hybridge rectifier. Even considering that there is about 15% step up in the transformers volume and that there is no disequilibrium among the inductors currents in the hybridge rectifier, one can see a considerable reduction in the total magnetic volumes.

III. EXPERIMENTAL RESULTS

In order to validate the theoretical assumptions, an experimental prototype was designed according the specifications and components presented in Tables III and IV.

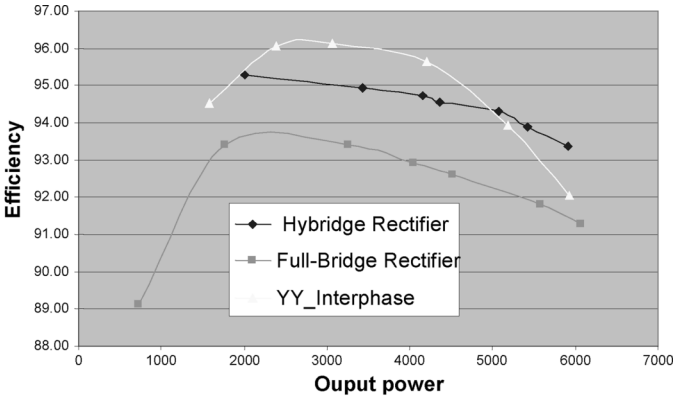

Fig. 22. Efficiency of the proposed converter compared to the hybridge and full-bridge topologies.

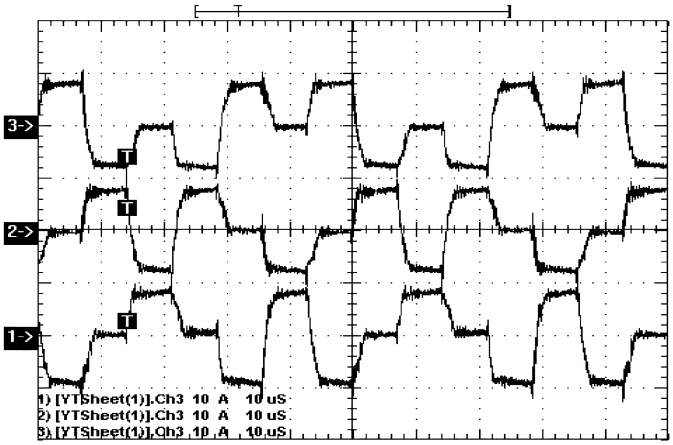

Fig. 23. Currents through primary windings for ($D = 0.98$(1 − i_{Lpa}; 2 − i_{Lpb}; 3 − i_{Lpc}; 10 A/div).

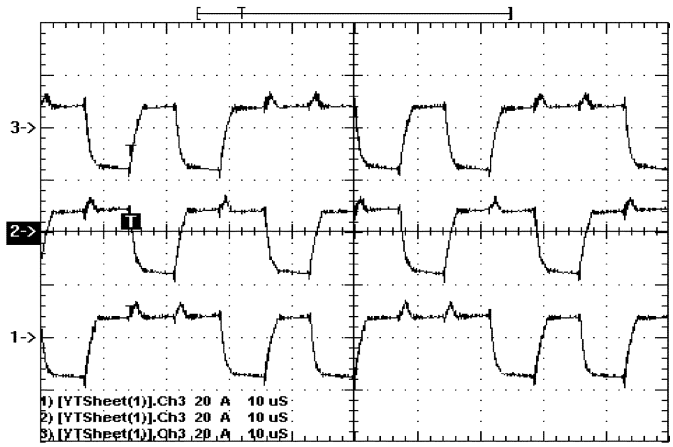

Fig. 24. Line currents (phase C—channel 1, phase B—channel2, phase A—channel 3) (20 A/div, 10 μs/div).

Fig. 22 shows the efficiency obtained for the proposed converter compared with other rectifier topologies [8], [10], as data were obtained in open loop situation. From this graph, it can be said that this is an intermediary solution, since efficiency is better than that in the full-bridge rectifier [8] but the increase in the global volume is not as large as in the hybridge rectifier [10]. In Fig. 23, currents through primary windings are depicted, where a satisfactory equilibrium among them is verified ($I_{Lpa} = 6.3$ A, $I_{Lpb} = 5.95$ A, $I_{Lpc} = 6.6$ A). Fig. 24 shows the line currents ($I_A = 10.7, I_B = 10.4$ A, $I_C = 10.3$ A).

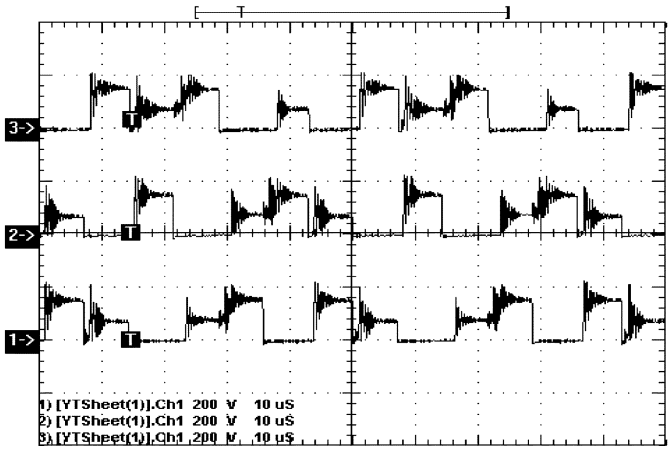

Fig. 25. Voltages across output rectifier diodes D_4, D_5, and D_6 (200 V/div—10 μs/div).

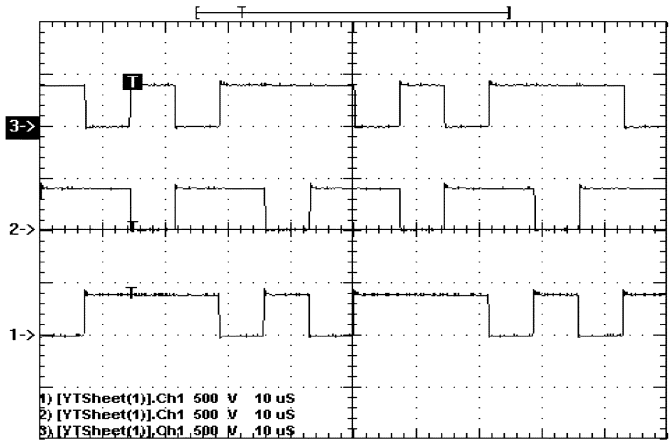

Fig. 26. Voltages across switches S_2, S_4 and S_6 (500 V/div, 10 μs/div).

Fig. 25 corresponds to the voltages across rectifier diodes D_4, D_5, and D_6, using RCD snubbers. Fig. 26 shows the voltages across switches S_2, S_4, and S_6.

The aforementioned results demonstrate the functionality of the converter for $D \cong 0.5$. However, the worst condition for disequilibrium in the output inductors currents i_{L01} and i_{L02} occurs when $D < 0.33$. Fig. 27 shows the currents through output inductors for $D = 0.21$. This important result demonstrates the ability of this converter to operate in Region 2, since the equilibrium between the inductors currents is maintained. Then, output voltage variation and control is possible.

IV. Conclusion

This paper has shown that the use of a three-phase dc–dc converter associated with a delta double-Wye connected rectifier with interphase inductors is able to control the output voltage, since the equilibrium between the output inductors currents is maintained within the complete operation range.

The operating stages and main waveforms were presented and analyzed. From the theoretical analysis, the cause of the disequilibrium between the output inductors current was elucidated. A

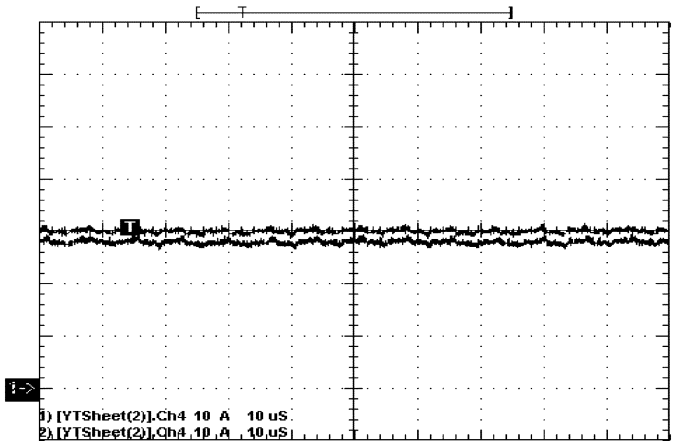

Fig. 27. Currents through output inductors i_{L01} and i_{L02} for $D = 0.21$ (10 A/div, 10 μs/div).

new modulation technique was then proposed and analyzed in order to mitigate such disequilibrium.

Experimental results and theoretical analysis showed that the proposed topology is an alternative for the three-phase dc–dc converter, since efficiency is better than that in full-bridge rectifier but the increase in the global volume is not as large as in hybridge rectifier.

All theoretical considerations were validated by simulation and the experimental results, obtained from a laboratory prototype of 6 kW.

REFERENCES

[1] I. Barbi and W. A. Filho, "A non-resonant zero voltage switching pulse width modulated full-bridge dc–dc converter," in *Proc. IECON*, 1990, pp. 1051–1056.

[2] R. L. Steigerwald and K. D. T. Ngo, "Full-Bridge Lossless Switching Converter," U.S. Patent 4 8644 79, Sep. 5, 1989.

[3] P. D. Ziogas, A. R. Prasad, and S. Manias, "Analysis and design of a three-phase off-line dc–dc converter with high frequency isolation," in *Proc. Ind. Appl. Soc. Conf.*, 1988, pp. 813–820.

[4] D. M. Divan and R. W. A. A. De Doncker, "A three phase soft switched high-power density dc–dc converter for high power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[5] A. K. S. Bhat and L. Zheng, "Analysis and design of a three phase LCC type resonant converter," in *Proc. IEEE 27th Annu. Power Electron. Spec. Conf. (PESC'96)*, Baveno, Italy, Jun. 23–27, 1996, vol. 1, pp. 252–258.

[6] P. D. Ziogas, A. R. Prasad, and S. Manias, "A three phase resonant PWM dc–dc converter," in *Proc. IEEE 22nd Annu. Power Electron. Spec. Conf. (PESC'91)*, Cambridge, MA, Jun. 24–27, 1991, pp. 463–473.

[7] N. Mohan and P. Imbertson, "Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty," *IEEE Trans. Ind. Appl.*, vol. 29, no. 1, pp. 121–125, Jan./Feb. 1993.

[8] D. S. Oliveira Jr. and I. Barbi, "A three-phase ZVS PWM dc–dc converter with asymmetrical duty cycle for high power applications," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 370–377, Mar. 2005.

[9] D. S. Oliveira Jr., I. Barbi, D. S. Oliveira Jr., and I. Barbi, "A three-phase version of the hybridge rectifier associated to the three-phase ZVS dc–dc converter with asymmetrical duty cycle," in *Proc. IEEE Int. Symp. Ind. Electron.*, Rio de Janeiro, Brazil, 2003, pp. 516–520.

[10] D. S. Oliveira Jr. and I. Barbi, "A three-phase version of the hybridge rectifier associated to the three-phase ZVS dc–dc converter with asymmetrical duty cycle," in *Proc. 34th IEEE Power Electron. Spec. Conf.*, 2003, vol. 2, pp. 616–621.

[11] S. Kim, "New multiple DC-DC converter topology with a high frequency zig-zag transformer," in *Proc. 19th Appl. Power Electron. Conf. Expo*, Houston, TX, 2004, vol. 1, pp. 654–660.

[12] J. Schaefer, *Rectifier Circuits: Theory and Design*. New York: Wiley, 1965.

[13] D. S. Oliveira Jr. and F. L. M. Antunes, "A novel modulation technique applied to the three-phase ZVS PWM dc–dc converter associated with a double-Wye connected rectifier, delta primary," in *Proc. 6th IEEE Int. Conf. Ind. Appl.*, Joinville, Brazil, Oct. 12–15, 2004, pp. 852–856.

[14] D. S. Oliveira Jr. and I. Barbi, "Dynamical analysis of the three-phase dc–dc converter with asymmetrical duty cycle, associated to a three-phase version of the hybridge rectifier," in *Proc. Brazilian Power Electron. Conf.*, Fortaleza, Brazil, 2003, vol. 1, pp. 65–69.

Demercil S. Oliveira, Jr. was born in Santos, São Paulo, Brazil, in 1974. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1999 and 2001, respectively, and the Ph.D. degree from the Federal University of Santa Catarina, Santa Catarina, Brazil, in 2004.

Currently, he is a Researcher in the Power Processing and Control Group, Federal University of Ceará, Ceará, Brazil. His interest areas include dc–dc conversion, soft commutation, and renewable energy applications.

Fernando Antunes (M'95) received the B.Sc. degree in electrical engineering and the B.Sc. degree in business and administration from Federal University of Ceará, Ceará, Brazil in 1978 and 1983, respectively, . In 1980 he received the M.Sc. degree from the University of São Paulo, São Paulo, Brazil, in 1980, and the Ph.D. degree in power electronics and machine drives from Loughborough University of Technology, Loughborough, U.K., in 1991.

He is a Senior Lecturer with the Federal University of Ceará where he coordinates the Power Electronics Group. His research fields include multilevel converters, inverters, and their application to renewable energy.

Dr. Antunes is member of the IEEE Power Electronics Society and the Brazilian Power Electronics Society (SOBAREP)

Carlos Elmano de Alencar e Silva was born in Ceará, Brazil, in 1981. He received the B.Sc. degree in electrical engineering from the Federal University of Ceará, Ceará, Brazil, in 2004 where he is currently pursuing the M.Sc. degree.

His research interests include dc–dc conversion, dc/ac conversion, and digital control.